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SEPT 3
Issue 18/2007
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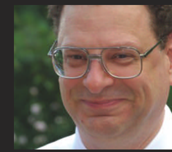

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FPGA-BASED DESIGN YIELDS LOW-COST ARBITRARY-FREQUENCY GENERATOR

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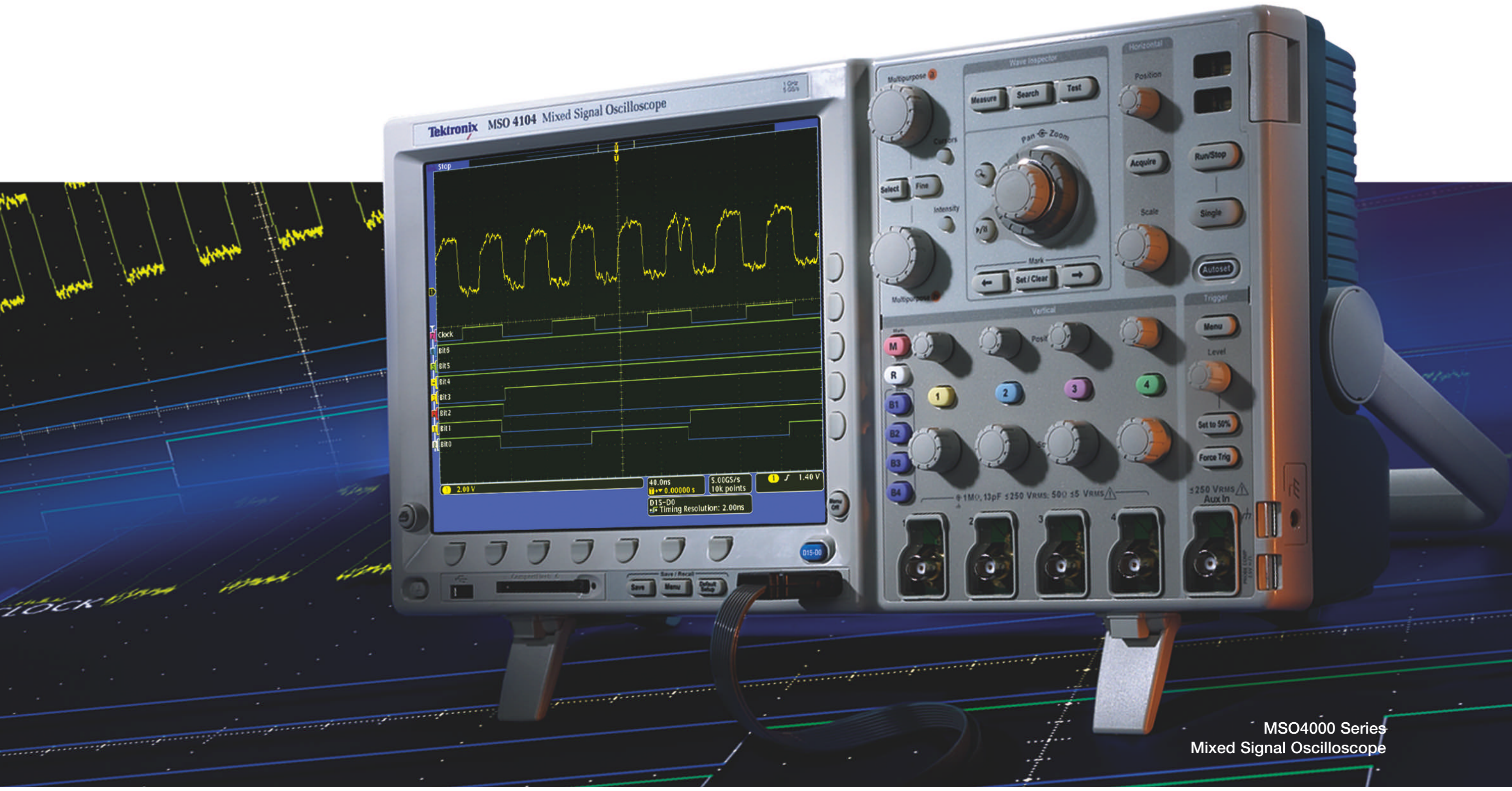
Mixed signals, one instrument.

A powerful oscilloscope with logic analyzer functionality.



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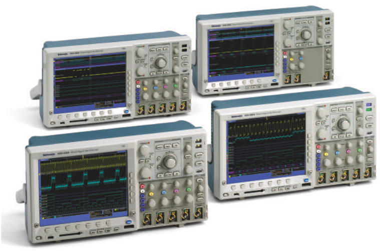

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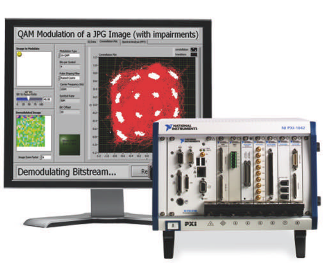

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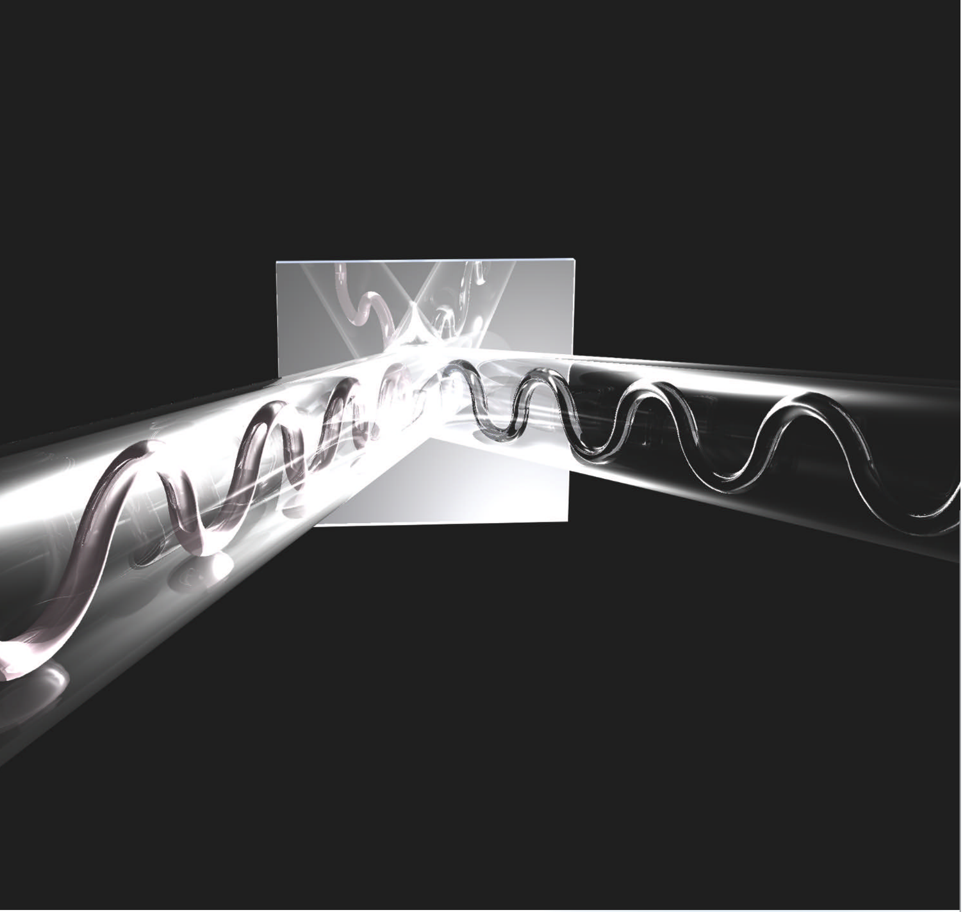

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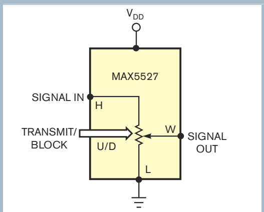

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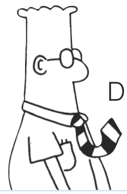

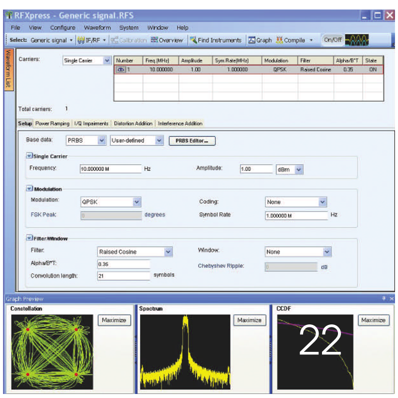

DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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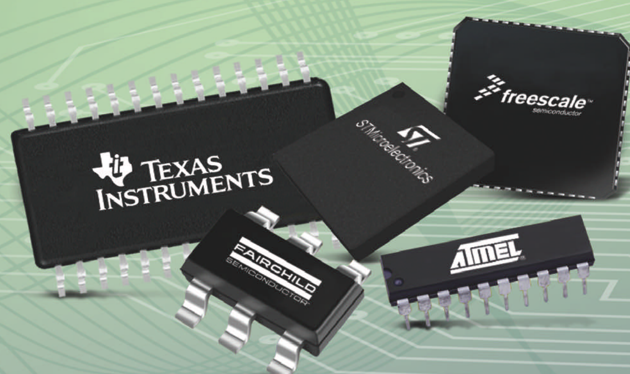

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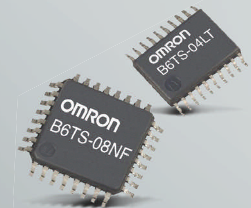

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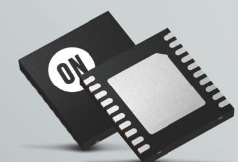

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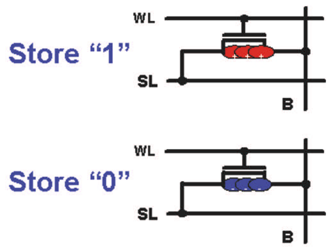

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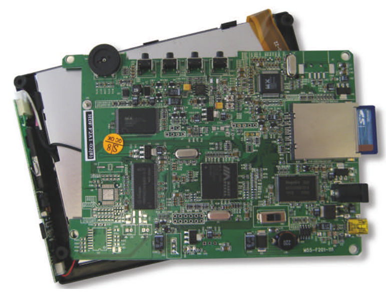

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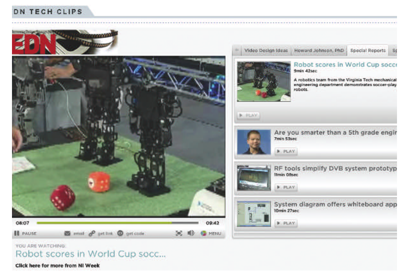

EDN TECH CLIPS

Check out the Tech Clips page for a panel discussion on the hazards of IP reuse, plus a series of technical demos from the recent National Instruments Week, including soccer-playing robots, a fifth-grade LabView expert, and algorithm engineering.
→www.edn.com/techclips

A BRIEF BRAG
EDN recently won three national “Azbee” awards from the ASBPE (American Society of Business Publication Editors). We received a silver award for last September’s special 50th Anniversary issue. Senior Technical Editor Brian Dipert won a gold for his popular blog, *Brian’s Brain*. And Art Director Mike O’Leary brought home a silver award for his “Mobile makeover” illustration (above).
50th Anniversary Issue
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Brian’s Brain
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“Mobile makeover” article
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FROM *EDN*’s BLOGS
Move over ZigBee, make room for 6LoWPAN

From Embedded Webblog, *by Warren Webb*
There’s a new kid on the networking block with an unusual name: 6LoWPAN, which stands for IPv6-based, low-power, wireless, personal-area network.
→www.edn.com/070903toc3

Functionality-rich Design for Consumer Electronics Made Easier

By: QuickLogic™

▶THE CHALLENGE

The consumer electronics market has never been more dynamic or better poised for growth. This is especially true for "must-have" gadgets like Portable Navigation Devices (PNDs) and Personal Media Players (PMPs). As stated by Gartner, in 2006, sales of PNDs in the United States stood at 3.5 million. This year that number is expected to reach 5 to 8 million. The outlook for PMPs looks just as promising with shipments in areas like China expected to reach 1.43 million by 2010.

With consumer electronic products, the key to commercial success lies in the ability to continually provide consumers with rich, flexible features and standards-based functionality. The challenge of integrating these features and emerging standards without jeopardizing performance, schedule, budget or power targets falls to the system designer.

▶THE SINGLE-CHIP SOLUTION

Helping designers handle these challenges is the new ArcticLink™ Solution Platform introduced by QuickLogic™ earlier this year. This family of low-power devices combines hardwired application-specific logic with an ultra-low power programmable fabric block all in a single-chip solution (see Figure 1). The combination of small form factor packaging, ultra-low power technology and host bus interface configurability makes this an ideal platform for addressing emerging connectivity requirements in power-critical mobile applications.

The highly **flexible** ArcticLink Solution Platform can implement configurable host controllers, while the programmable fabric can be tailored for custom functions or additional connectivity requirements. QuickLogic offers a diverse portfolio of pre-verified modules such as Hi-Speed (HS) USB 2.0 OTG, SD/SDIO/MMC/CE-ATA, NAND flash, IDE/ATA, PCI, Bluetooth 2.0 UART, SPI and several others. In addition, the programmable fabric allows for seamless connectivity to any application processor. The ArcticLink Solution Platform's **ultra-low power** status comes from its Very Low Power (VLP) mode, which shuts down the chip when it's not in use.

This solution has a level of integration allowing for the replacement of up to 5 discrete components in a single design, resulting in a significant **reduction in board space**. The ability to add functionality to a design without changing the processor is a noteworthy benefit of the ArcticLink Solution Platform that helps with **longevity**. The programmable fabric allows designers to create multiple spins to accommodate next generation products, providing the additional benefit of cost savings. Finally, from the system's design perspective, the ArcticLink Solution Platform helps **minimize risk**, both through its use of verified, embedded IP, and its support for design reuse.

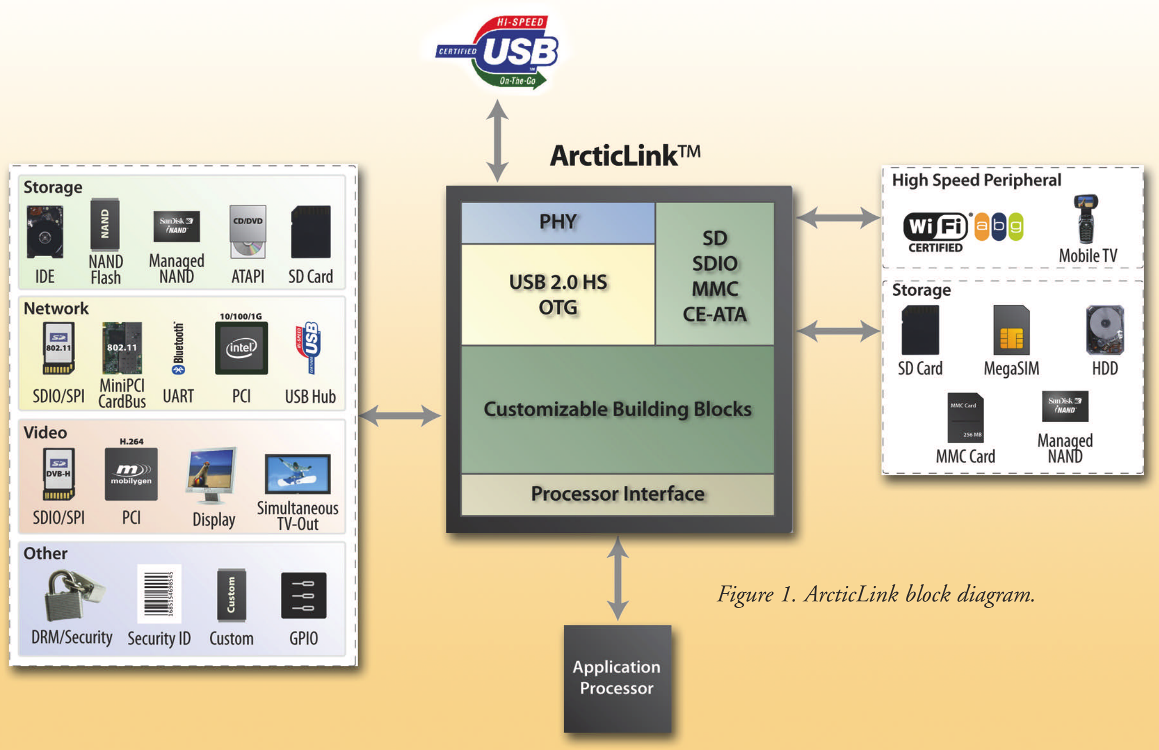

Figure 1. ArcticLink block diagram.

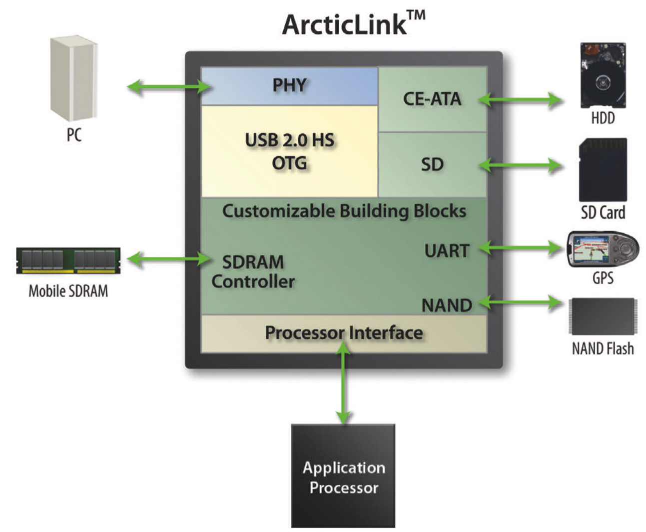

Figure 2. Smartphone design example.

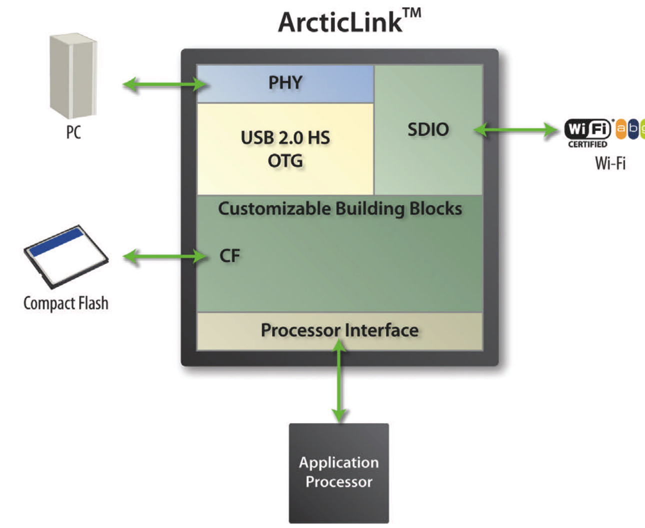

Figure 3. PMP design example.

▶DESIGN EXAMPLES

The ArcticLink Solution Platform is ideal for accelerating time-to-market, and aiding differentiation in the marketplace. The examples below showcase the features and benefits listed above.

Feature-rich Smartphone Design *(see Figure 2)*
In this smartphone design, ArcticLink's flexibility, small form factor and high level of feature integration were key. For this design, requiring USB 2.0, CE-ATA, SDIO, a microprocessor and a memory interface, ArcticLink was able to replace all 5 components. This not only saved valuable board space, but did it without compromising the power budget.

Shortened PMP Design Cycle *(see Figure 3)*
In this PMP application, low-power, a small form factor and a short design cycle were the critical elements. Compact Flash, USB and a microprocessor were all replaced by the ArcticLink Solution Platform. The USB 2.0 was delivered with drivers, and all required software, which helped significantly shorten the design cycle. QuickLogic offers the complete solution package, and above all provides the low-power critical for a mobile application. ■

PROFILE QuickLogic Corporation

QuickLogic Corporation NASDAQ: QUIK) is the leading provider of the lowest power programmable solutions for the portable electronics, industrial, communications and military markets. Our latest products, ArcticLink™, PolarPro™, Eclipse II™ and QuickPCI™ are being used to implement bridge and control solutions in embedded systems requiring Wi-Fi, DVB-H and IDE or CE-ATA-based disk drives. QuickLogic's proprietary ViaLink® technology offers significant benefits for programmable logic, including the lowest power, instant on capability and unmatched intellectual property security. The company is located at 1277 Orleans Drive, Sunnyvale, CA 94089-1138. www.quicklogic.com

BY MAURY WRIGHT, EDITORIAL DIRECTOR

Immaturity in 802.11n products guides a return to a wired LAN

I recently bought a Draft-n-compliant wireless router but was extremely disappointed in the performance. The event revamped my thinking about the "IT" infrastructure in my home. And it made me wonder how many people might come to the same question that perturbed me: Does integrating wireless support in a router make sense?

I've written regularly about the need for a multimedia-capable home network. And going back more than five years, I've regularly stated that range is often more important than speed in wireless-networking products. I've certainly hoped that 802.11n would finally deliver the speed necessary for video along with whole-house coverage.

I had for a couple of years been happily using a Belkin router based on an early MIMO (multiple-input/multiple-output) chip set from Airgo Networks (now part of Qualcomm). In my test, that product bested all other 802.11 products that I had tested in offering the range to cover my entire home and yard (www.edn.com/article/CA6296066).

Recently, however, my son bought a Nintendo Wii console. The Wii includes an 802.11g client but not a wired-Ethernet port. The Wii didn't connect with the Belkin router. A little Web research revealed a number of wireless issues with the Wii and the fact that the Belkin router was one of a few products that absolutely doesn't work with the Wii.

I figured it was time for an upgrade, anyway. I had recently discussed Draft-n products with Broadcom and even written a column about the conversation (www.edn.com/article/CA6434332). Broadcom had assured me that its Draft-n chips would be software-upgradable to the 802.11n standard and that it was matching the performance of Airgo-based routers—which are really 802.llg extenders, because the shipping products don't follow the Draft-n path. So, I bought a $99 Linksys WRT150N router with an integrated Ethernet switch that I'm fairly sure uses a Broadcom chip.

A wired-only router may seem like a step backward, but it feels more like a step forward.

The performance was miserable. With the router in my office, I couldn't get a reliable signal in my living room on the Wii or my notebook PC. A quick search of reviews on the Internet (yes, I should have done that research first) revealed that all of the Draft-n products perform poorly. So, I returned the Linksys router.

I spent a few days researching my next move. Ironically, the RangeMax 240 that Netgear announced a while ago seems to be the top-performing product. It uses Airgo's third-generation MIMO chip. But it no longer seems to be on the market. I did consider other wireless routers; then, while standing in an aisle at Best Buy, it hit me that I should just buy a wired router with a GbE (gigabit-Ethernet) switch.

I did a bit of research on wired routers. Inexpensive options with 100-Mbps Ethernet abound. But, if I was going to separate my wired and wireless networks, I felt that a product with a long life expectancy was essential. So, I paid $129 for a Linksys RVS400 with a four-port GbE switch. The product appears to target small businesses more than home users. It comes in business attire rather than the loud purple package of most Linksys products. And it offers far more features in VPN (virtual-private-network) support and configurability.

I had a Category 5 link to my living room and a switch there to connect the Xbox 360 and the SlingBox. I went to Fry's and bought one of its loss-leader, generic 802.11g access points for $25. The user interface for the Airlink access point isn't as slick, but it is up and working just fine. The Wii and my son are happy. The access point in the center of my house seems to be providing good coverage wherever I need it.

I figure I'll sit out the first round of 802.11n products. A wired-only router may seem like a step backward, but it feels more like a step forward now that it's up and working. And I'll recoup the investment in GbE over time. I won't need to replace the wired router for years, and I can change the access point when better options become less costly. And, if I were a router vendor, I'd design products thinking that other customers might make the same decision I made. EDN

Contact me at mgwright@edn.com.

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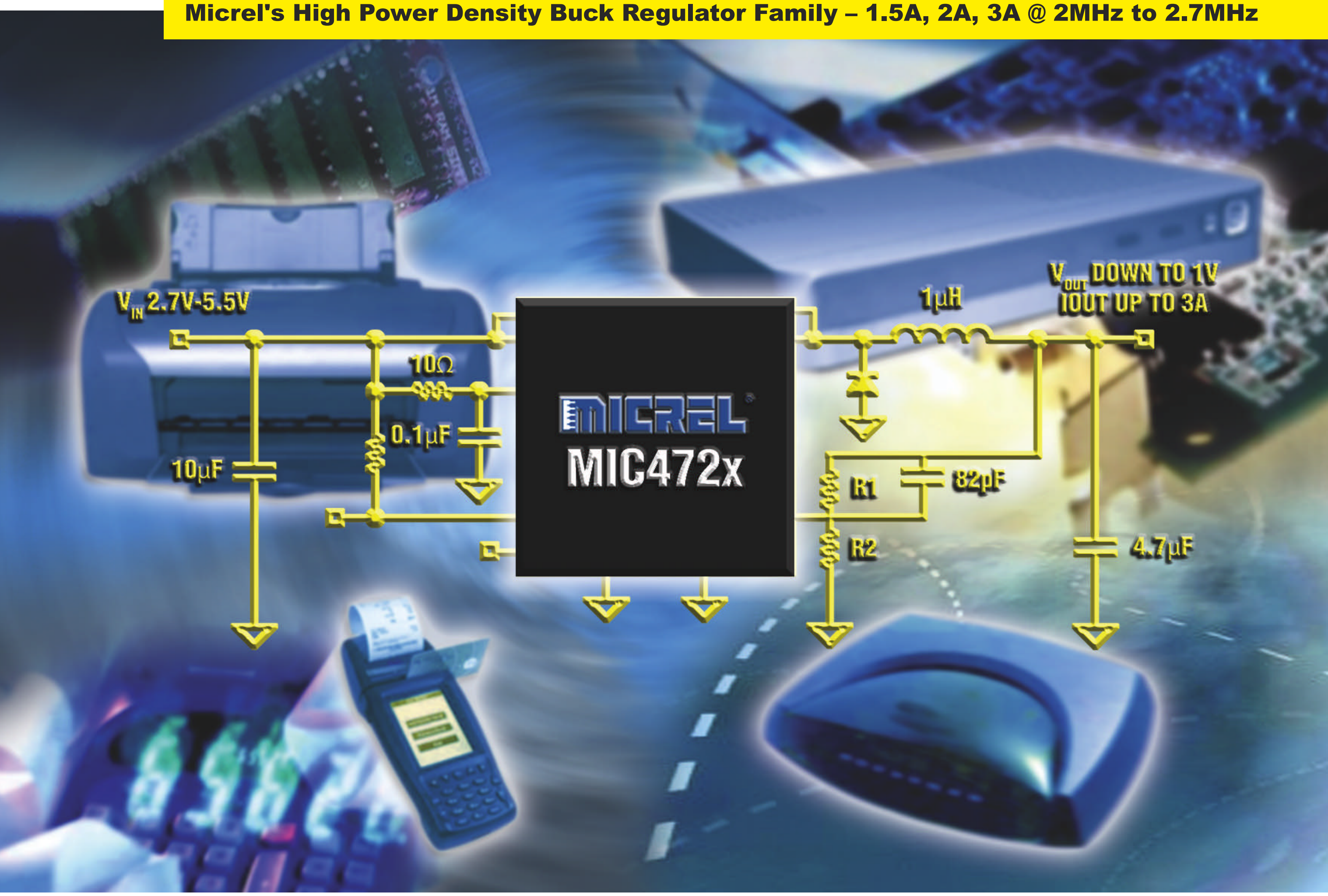

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Saving Power in an AC-Coupled Amplifier Circuit

Application Note AN-1684

Carine Alberti, Applications Engineer

AC-coupled circuits are often used for single-supply operation to bring the input voltage into the input range of the amplifier. This circuit topology can be used in AC smoke detectors or in AC proximity sensors. *Figure 1* shows an AC-coupled inverting-amplifier circuit.

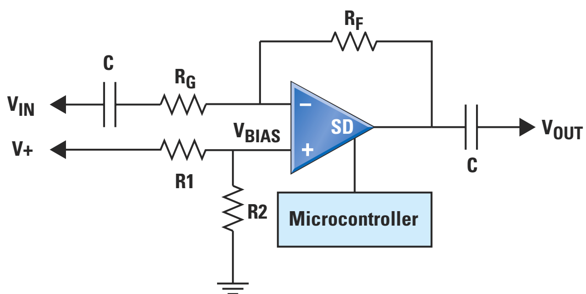

Figure 1. AC-Coupled Inverting Amplifier with Shutdown Pin

In the previous circuit, the non-DC input voltage is multiplied by the desired negative gain as follows:

$$V_{OUT} = -\frac{R_F}{R_G} \text{ x } V_{IN} + V_{BIAS}$$

The biasing voltage (V_{BIAS}) is half of the supply voltage (V+) and is added to the non-inverting input to bring the input voltage within the normal operating range of the amplifier. It also provides an offset for the output so that it is within its operating range.

In battery-operated circuits such as a smoke detector, an effective way to save power is to power down the circuit for a few seconds, and only sense smoke for a few microseconds. Usually when power saving is necessary, the conventional implementation is to power off the circuit by using an amplifier with a shutdown pin. This method has the disadvantage of allowing the coupling capacitors to discharge during the shutdown state. When the amplifier is turned on again, the circuit needs to reestablish the quiescent DC voltages. During this time, the amplifier's output is not usable because the output signal is a mixture of the amplified input signal and the charging voltage on the coupling capacitors. And the settling time can range from several microseconds to several milliseconds, depending on the resistor and capacitor values.

LPV531 Programmable Amplifier

The LPV531 programmable operational amplifier is ideal for AC-coupled circuits; its programmable-power mode allows the circuit to be kept active to maintain, in low-power mode, a quiescent charge on the coupling capacitor. The advantage of this method is the reduction of time needed to reestablish a quiescent operating point when the amplifier is switched to full-power mode.

The LPV531 op amp offers the capability to adjust the supply current, which is made possible by the I_{SEL} control pin. The supply current is 40 times higher than the I_{SEL} current. The maximum current that can flow from the I_{SEL} pin is determined by an internal 110 mV reference voltage, and an 11 kΩ internal resistor. The supply current can be reduced by connecting an external resistance to the I_{SEL} pin.

$$Is = I\ \mu A + 40 \text{ x } \frac{110\ mV - V_{CONTROL}}{R_{EXT} + 11\ k\Omega}$$

Figure 2 shows an example of how to control the supply current.

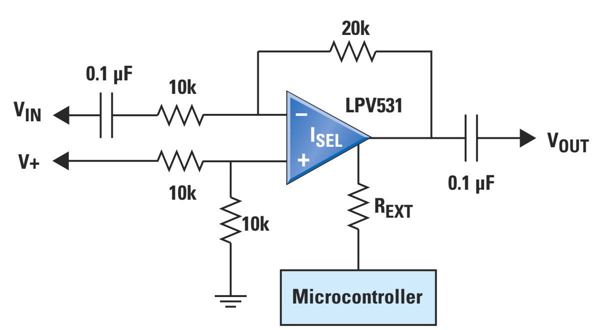

Figure 2. AC-Coupled Inverting Amplifier with the LPV531 Amplifier

National Semiconductor
The Sight & Sound of Information

The power mode of the amplifier can be controlled by the microcontroller. By increasing the control voltage up to 110 mV, the supply current of the amplifier will decrease. Therefore it is possible to choose between a full-power mode and a low-power mode, while maintaining an active circuit. ***Figure 3*** illustrates the relationship between the control voltage and the supply current of the amplifier.

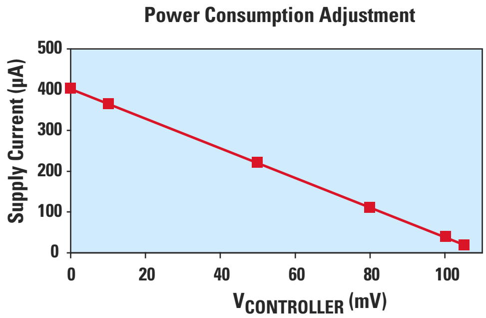

Figure 3. Power-Mode Control (R_{EXT} = 20Ω)

Faster Settling Time with the LPV531 Amplifier

Comparing the results obtained with the LPV531 op amp and an amplifier with shutdown mode such as the LMV981 will further illustrate the much shorter settling time. ***Figure 4*** shows the measurement obtained with the LPV531 amplifier.

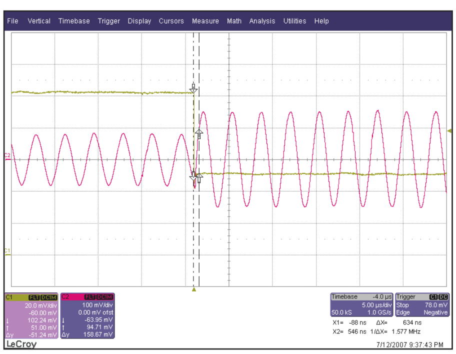

Figure 4. Output Signal with the LPV531 Op Amp

The yellow line is the control voltage. When the control voltage passes from high level to low, the amplifier switches to full-power mode. As ***Figures 3*** and ***4*** indicate, we can estimate that for a control voltage of 105 mV (low-power mode), the supply current is 20 µA. For a control voltage of 55 mV (high-power mode), it is 200 µA. The yellow signal is the output signal, where we can estimate that the settling time to obtain a stable signal is around 634 ns.

Figure 5 shows the results obtained with the LMV981 amplifier featuring a shutdown pin. The voltage applied on the shutdown pin is the yellow signal. To shut down the LMV981 amplifier, the turn-off voltage is 0.55V. The turn-on voltage to enable the device is 1V.

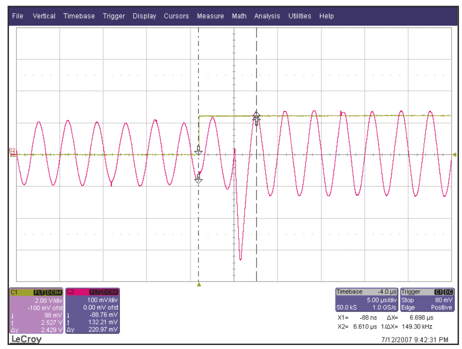

Figure 5. Output Signal with an Amplifier with Shutdown

The measurement illustrates the fact that the set-up time is really longer with this kind of circuit. The circuit needs approximately 6.7 µs to be stable, which is ten times more than the circuit using the LPV531 op amp. During this settling time, the output signal is not usable.

Conclusion

This article has shown that the LPV531 amplifier is ideal for use in AC-coupled applications to reduce the settling time of the output signal by maintaining a quiescent charge on the capacitors. For battery-operated applications which are non-AC coupled, the LMV981 amplifier is a very good choice. This amplifier can be supplied from 1.8V to 5V, has a supply current of only 100 µA, and has rail-to-rail input and output. ■

For Additional Design Information

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National Semiconductor
The Sight & Sound of Information

Audio, video chips enhance handheld devices' features, shrink power needs

A handheld consumer device's display and audio are often the features that determine the product's success or failure. However, audio and video bells and whistles can also destroy a battery-operated device's power budget. So, you should spend some serious design time selecting and designing audio and display capabilities for your next handheld product. To help you with those designs, National Semiconductor has introduced a suite of display, audio, and power-management ICs that conserve space and power in handheld multimedia-enabled devices, and the products streamline the design of these features.

For example, you may assume that the most efficient way to backlight a handheld display is with a white LED, but this approach isn't necessarily the best choice for today's high-definition, full-color handheld displays. Mark Davidson, marketing director for the power-management division for National Semiconductor, points out that so-called white LEDs vary in their whiteness, which changes over time. If you lock yourself into a single, fixed-color white LED for illumination, you thus give up the ability to compensate for LED aging, as well as variability in display color. National Semiconductor's new LP5520 RGB LED driver, with prices starting at 90 cents (1000), tunes three RGB LEDs to produce a true white light over a wide temperature range without the need for optical feedback. But you still must allow for individual screen and LED characteristics: For example, you might need to use various vendors' LEDs and screens, all with different aging characteristics. So, National Semiconductor also offers the $3.40 (1000) FPD95120 LTPS (low-temperature-polycrystalline-silicon) display driver, which includes an EEPROM. You can use the driver with multiple manufacturers' displays because the EEPROM stores module-calibration data to match color and flicker parameters and provides the ability to program unique product identification.

> "Processors that incorporate PowerWise intellectual property adaptively adjust the supply voltage to the minimum necessary level.

Video processing represents another significant portion of a device's power budget. The LP5552 power-management IC supports AVS (adaptive voltage scaling) to enable processors that incorporate National Semiconductor's PowerWise intellectual property to adaptively adjust the supply voltage to the minimum necessary level. Available in a 36-bump micro-SMD package, the $4.50 (1000) LP5552 includes two 800-mA buck regulators and five LDO (low-dropout) regulators.

Audio quality is just as important as video in defining a device's quality. The LM49100 audio chip routes monophonic-voice or stereo-music signals to a mono-speaker driver or stereo-ground-referenced headphone amplifiers through preset modes. It also provides layout flexibility through its headphone's ground-sensing function. To maximize battery life, the $3.35 (1000) LM49100 has a quiescent current of less than 5 mA with all channels active.

—by Margery Conner

▷**National Semiconductor**, www.national.com.

Measuring just 0.9 mm wide, the FPD95120 display driver lets designers maximize the active area of the display glass. The driver provides a deserializer; a high-efficiency, inductive dc/dc switcher; and RAM to enable standby, low-power-display capabilities.

FEEDBACK LOOP

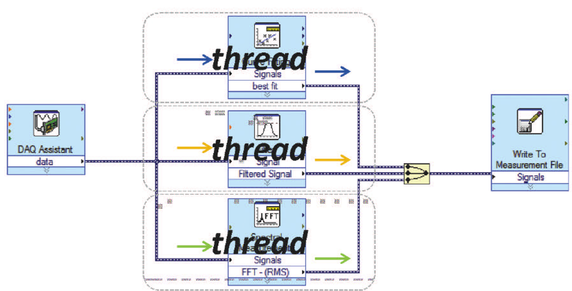
"Power cords actually do sound different. Granted, the excuses marketing departments come up with sound good only to the lay person. And, yes, the goal is to make exorbitant profits on something as simple as wire. Granted, wire is just wire. But my life (and job) would be a lot easier if it all sounded alike."

—Reader Pat Di Giacomo gives his opinions in *EDN*'s Feedback Loop, at www.edn.com/CA6418215. Add your comments.

LabView V8.5 adds state charts, enhances multithreaded-application performance in multicore microprocessors, FPGAs

Amid the traditional annual fanfare of NI-Week in its home city of Austin, TX, National Instruments has announced Version 8.5 of LabView, the company's graphical system-design-software platform for test-, control-, and embedded-system development. With its parallel-data-flow language and intuitive graphical approach to multithreading, Version 8.5 simplifies development of multicore- and FPGA-based applications. According to NI, as IC manufacturers turn to parallel-multicore architectures to improve microprocessor performance, running these new processors under LabView 8.5 will enable system developers to achieve faster throughput, more efficient processor-intensive analysis, and more reliable real-time operation with little or no change to applications. Version 8.5 also extends LabView further into embedded and industrial systems with a new state-chart-design module for modeling and implementing system behavior and with new I/O libraries and analysis functions for industrial monitoring and control.

The adoption of next-generation processors requires system developers to consider how their software can realize multicore- and FPGA-based systems' potential for improved performance. NI says that LabView's parallel-data-flow language helps users to map their applications to such new architectures. Building on the automatic-multithreading capability of earlier LabView versions, Version 8.5 scales user applications based on the total number of available cores and delivers enhanced thread-safe drivers and libraries to improve throughput.



Although LabView has supported multithreading for nearly a decade, its ability to handle multiple threads in multicore processors is more recent, and Version 8.5 incorporates many new features that further optimize application performance in systems based on such processors.

The new version's real-time environment also delivers SMP (symmetric multiprocessing), through which embedded- and industrial-system designers can automatically load-balance tasks across multiple cores without sacrificing determinism. To fine-tune real-time systems or isolate time-critical code segments on a dedicated core, application developers can also manually assign portions of code to specific cores. To meet the challenges of debugging and code optimization in real-time-multicore systems, developers can use the new Version 2.0 Real-Time Execution-Trace Toolkit to visually display timing relationships between code segments and the individual threads and cores in which the code executes.

LabView's inherent parallelism also suits it for developing FPGA-based applications. Version 8.5 continues to simplify FPGA programming with an enhanced project wizard that automates I/O configuration; IP (intellectual-property) development; and setup of common I/O, counter/timer, and encoder applications. Using this wizard, developers can automatically generate complex high-speed DMA (direct-memory-access) data-transfer code. In addition, LabView 8.5 offers multichannel filtering and PID (proportional/integral/derivative)-control functions that significantly reduce the FPGA resources in high-channel-count machine-automation applications.

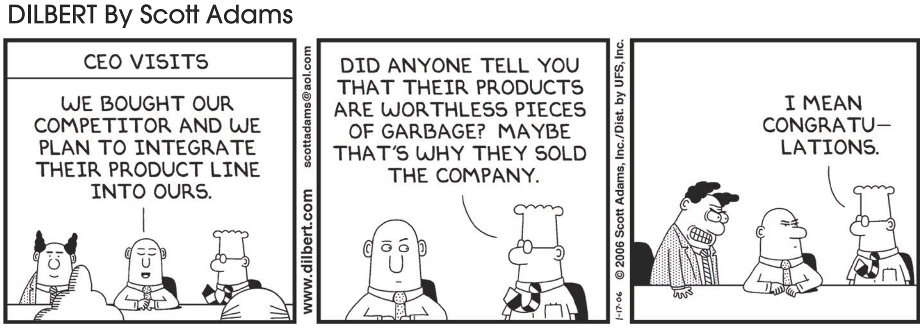
Engineers commonly use state charts to design state machines that model the behavior of real-time and embedded systems—for example, to depict event occurrences and responses in digital-communication protocols, machine controllers, and system-protection applications. LabView 8.5 adds a new state-chart module to help developers design and simulate these event-based systems using familiar, high-level state-chart notations based on the UML (Unified Modeling Language) standard.

Because the LabView State-Chart Module is based on the LabView graphical-programming language, developers have a unified platform for quickly designing, prototyping, and deploying their systems and combining familiar state-chart notation with real-world I/O running on deterministic real-time- or FPGA-based systems. The US price for LabView 8.5 begins at $1199.

—by Dan Strassberg

▷**National Instruments**, www.ni.com/labview85.

DILBERT By Scott Adams



Software simplifies use of AWGs for digital-RF testing

Tektronix has announced RFXpress, a software package for creating and editing digitally modulated RF (radio-frequency)-, IF (intermediate-frequency)-, and IQ (in-phase/quadrature)-signal waveforms, which the company's AWG5000 and AWG7000 AWGs (arbitrary-waveform generators) can reproduce. The software provides an intuitive user interface that, according to the company, greatly simplifies creating and managing general-purpose digital-RF waveforms. The package also accommodates specialized UWB (ultrawideband)-WiMedia plug-in software modules and a library of waveforms for thoroughly testing new digital-RF designs.

Signal generation for stress testing of new-product designs is a critical step in the development of modern wireless devices. Historically, generating such signals has been complex, often requiring many hours of tedious setup of multiple instruments. RFXpress simplifies the task by automating many repetitive and arcane functions. "Instead of creating mathematical formulas, users of the general-purpose version of RFXpress need only provide information on such parameters as frequencies and modulation schemes to predefined, fill-in-the-blanks templates," says Mike Higashi, vice president of Tektronix's signal-source-product line. "Moreover, the compliance and custom plug-ins add capabilities that assist in reliably and efficiently performing a wide range of tests for the UWB WiMedia standard."

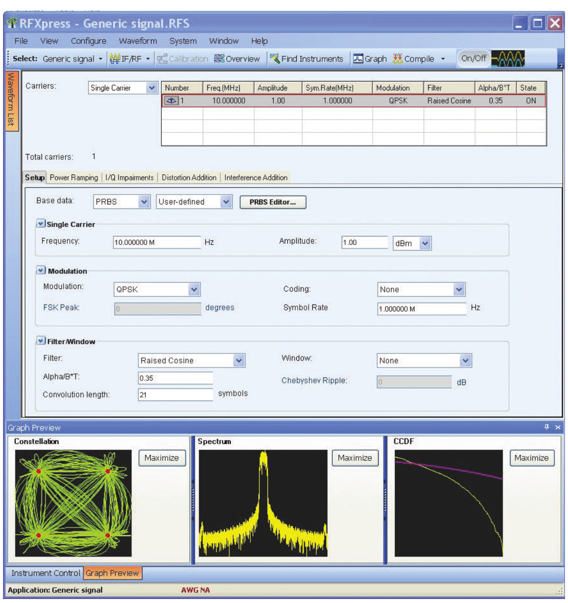
RFXpress, which supports a variety of modulation schemes, such as QPSK (quadrature phase-shift keying), QAM (quadrature-amplitude modulation), and GMSK (gaussian minimum-shift keying), also allows engineers to build their own modulation schemes. Furthermore, before you use an AWG7000 or an AWG5000 to replay RF, IF, and IQ signals captured on an oscilloscope or a Tektronix real-time spectrum analyzer, you can now use RFXpress to add impairments, interference, and distortion.

For many applications, RFXpress in combination with the AWG platform's inherent direct-synthesis capabilities enables simpler test setups that use fewer instruments than did earlier approaches. Direct synthesis is a flexible method for creating repeatable ideal and impaired waveforms that an AWG can then directly synthesize. For example, the RFXpress WiMedia custom-mode plug-in enables engineers to individually configure every part of the WiMedia frame and packet to thoroughly characterize, limit-test, and stress-test the receiver's PHY (physical) layer.

RFXpress runs as an integral part of the AWG5000 or AWG7000 or as a stand-alone application on an external PC. The suggested US price for general-purpose RFXpress is $5000. The UWB WiMedia-compliance plug-in costs $2200, and the UWB WiMedia custom plug-in costs $7200.

—by Dan Strassberg

▷**Tektronix Inc,** www.tektronix.com.



RFXpress software can show a digitally modulated RF signal as a constellation, a spectrum, or a CCDF (complementary cumulative-distribution function). The three views appear from left to right at the bottom of this display.

09.03.07

CESI PARTNERS WITH TEKTRONIX TO ESTABLISH RESEARCH LAB

Tektronix Inc has announced a partnership with the CESI (China Electronics Standardization Institution) to set up a joint lab for advanced research and assessment of digital-RF and DTV (digital-TV) standards in China. The new lab will be a key research facility for the development of China's new DTV and digital-RF standards. Tektronix will provide the newly established joint lab with its latest enhanced-video and RF-test instruments, including the PQA500 picture-quality analyzer, WVR7120 waveform rasterizers, and RSA6100A real-time spectrum analyzers.

The state-operated CESI is responsible for standardization and conformity assessment for the IT industry in China. CESI carries out tests, inspection, and certification of Chinese IT products and related equipment on behalf of the Chinese government. CESI's partnership with Tektronix is a part of its effort to address industry demands. The joint research lab will enable CESI to better manage the complexity of the latest high-speed circuitry and protocols, saving engineering time and achieving more reliable results.

"Tektronix is committed to working in partnership with China as the country continues to focus on transforming itself into an 'innovation nation' and empowering its engineers through our technology and products to develop solutions for the new digital world we live in," says Neil Huddlestone, president of Tektronix China. "This laboratory will play a key role in enabling the development of new Chinese standards and innovative products."

—by Fran Granville

▶**Tektronix**, www.tektronix.com.

GLOBAL DESIGNER

BY GRAHAM PROPHET

Waveform filtering shapes motor-drive currents

Epcos designed its SineFormer filter technology to improve the output waveforms from high-power frequency converters and motor drives. The unit simultaneously converts phase-to-phase voltages into a sinusoidal signal, damps common-mode currents, and forms the phase-to-ground voltage into a sine-shaped voltage. The technology suppresses voltage peaks that are harmful for motor windings and reduces bearing currents to negligible levels, thus significantly increasing the operating life of motors. Epcos officials say that cost savings in power-drive applications are also significant. The technology practically eliminates EMC (electromagnetic-compatibility) problems, so motors incorporating the filter do not require expensive, shielded motor cables or special cable ducts.

The company says that unshielded cable lengths of 1000m can comply with Class A, Group 1 EMC limits. And, because unshielded cables are more flexible, installation expenses are lower. Through the use of unshielded motor cables alone users can realize overall cost savings starting with cable runs of 100m. SineFormer requires no forced ventilation and is stable without a feedback loop to the converter-dc link. The unit is available in 520V-ac-rated voltage versions with rated currents as high as 180A and in 600V-ac versions with rated currents of 320A. The Underwriters Laboratories and CSA International approve all versions operating as high as 180A. Epcos plans to introduce further variants with rated voltages of 690V ac and rated currents as high as 1000A.

▷**Epcos**, www.epcos.com.

SineFormer improves output waveforms from high-power frequency converters and motor drives.

Low-power dc/dc downconverters target portable designs

Texas Instruments designed its TPS622xx series of 2.25-MHz-switching-frequency dc/dc step-down converters to power microcontrollers and DSPs in portable electronics. In three versions, the TPS62290, TPS62260, and TPS62240 provide 1A, 600 mA, or 300 mA, respectively, at output voltages as low as 0.6V±1.5% from an input voltage of 2.3 to 6V. They occupy a six-pin, 2×2-mm package; a minimal-area converter based on the 62260 uses 21.5-mm^2 board space with the addition of a 2.2-μH inductor, a 4.7-μF input capacitor, and a 10-μF output capacitor. The input voltage can be either a single lithium-ion cell or three alkaline cells. The converter, which operates at a 15-μA quiescent current, enters a power-save mode during light-load operating conditions and maintains efficiency as high as 95% over the entire load-current range. For low-noise applications, you can force the device into fixed-frequency PWM (pulse-width-modulation) mode by pulling the mode pin high. In the shutdown mode, the TPS62290's current consumption is less than 1 μA. The devices cost 95 cents, $1.20, and $1.75 (1000) for the TPS62240, TPS62260, and TPS62290 versions, respectively.

▷**Texas Instruments**, www.ti.com.

DRAGONFIRE REFERENCE DESIGN GETS BSP

EBV Elektronik and Domologic have announced a BSP (board-support package) for the Freescale (www.freescale.com)-microprocessor-based DragonFire reference design. The companies based this package on JControl technology; it allows designers to perform applications for the Cobra 5329 board in Java, simplifying development of GUIs (graphical user interfaces). The Cobra 5329 reference board uses the MCF5329 DragonFire 32-bit ColdFire microprocessor with the 240-MHz V3 core for monitoring and control applications with built-in graphics, such as measuring devices or control terminals. All members of the family have an SVGA LCD controller, a USB host and USB OTG (On-The-Go), an SDRAM controller for two memory banks, a 16-channel DMA controller, three UARTs, a queued SPI (serial-peripheral interface), and other peripheral elements. The Cobra 5329 has 16 Mbytes of SDRAM; 16 Mbytes of flash; and RS232, Ethernet, POE (power-over-Ethernet), and other interfaces.

JControl features short start time, low system requirements, a high degree of scalability, and easy adaptability to other display technologies. EBV says that the Cobra 5329 requires less than 2 seconds with JControl to finish setting up the GUI after power-up and short switching times from one monitor to another. The JControl/IDE (integrated development environment) runs on Windows and Linux and includes a built-in simulation environment; editors for fonts with support for non-Roman languages, such as Chinese and Japanese; pictures; and music. It also includes an optional, easy-to-use editor that allows you to create GUIs within a matter of minutes. You can add, scale, color, and write in new graphic components with no more than a few clicks of the mouse. A demonstration version is available for downloading.

▶**EBV Elektronik, www.ebv.com.**

▶**Domologic, www.domologic.com.**

09.03.07

VOICES

IBM's Jeffrey Taft: bringing intelligence to the power grid

PHOTO COURTESY FELICIA BROWELL

Jeffrey Taft is chief intelligent-grid architect for IBM's Global Business Services. As such, his background in digital-signal processing is vital as he heads up IBM's effort to become the purveyor of the software that runs the enormous distributed-processing network underlying the intelligent-power grid. *EDN* asked Taft about what the intelligent grid entails, what the benefits are to businesses and consumers, and how digital-signal processing plays a role in delivering power to consumers.

Just what *is* the intelligent grid?

A First, let's talk about the grid as it exists right now: You have a distributed infrastructure that includes power-generating stations, high-voltage transmission lines to carry bulk power out to delivery points, substations to break that power down to lower voltages, feeder circuits that run out to neighborhoods, and then distribution transformers to step the voltage down some more so that it's suitable for your house. Currently, your utility probably finds out about a power outage only after enough users call in. An intelligent power grid adds instrumentation to the grid devices, to the substations, and to the lines themselves, and it collects massive amounts of data and then processes the data so that it can be acted upon in an automated fashion.

What does all this intelligence mean to the residential or industrial consumer?

A There are several dimensions to the benefits of having an intelligent grid; some have a direct impact, and some are behind the scenes. Let's talk about customer impact: Would you like to be able to know when your power is more or less expensive and be able to optimize your usage based on that visibility? Would you like to know that, during certain hours of the day, your power is more expensive? Would you like to have your utility call you and tell you that the power is off at your home or facility and allow you to take early steps? Would you like to not even experience an outage because the utility had a way to head it off before it ever even happened? These capabilities are all available with an intelligent grid.

Why do the utilities want to move to the smart grid?

A Once the utility adds distributed sensors to the transmission-and-distribution system, it can automatically analyze all of that data for control purposes, for asset monitoring, for power-quality monitoring, and for outage intelligence. Rather than rely on customers to alert it to power outages, the utility will know exactly where the outage is, what equipment is affected, and what the root cause is and automatically dispatch the repair crew. But, even before the crew leaves, you'd like to isolate that fault with automatic switching and get as many customers as possible back online by rerouting power around the problem. The intelligent grid can do all that.

You're an electronics engineer with a strong background in digital-signal processing. How does that background help you build a smart power grid?

A There are a lot of parameters that you have to derive from basic waveform data. The power-distribution system is a three-phase system with complex connections. Its waveforms should nominally be simple sine waves, but, of course, in practice, they're not, and you have to do sophisticated signal processing just to extract the parameters that tell you what's going on. Through digital-signal processing, we get the information that tells us the real and reactive power flow that detects and locates problems in fault signatures and event correlations. We can tie that data together across multiple sensors and multiple power lines.

For example, an ordinary circuit breaker can operate multiple times to see if a fault is going to "self-heal." Let's say a branch falls and shorts out two power lines. The short may be temporary and burn away; you don't want to trip a circuit breaker and lose power due to a temporary glitch. So, the circuit breaker opens up the circuit, waits, closes it, and sees if power is there. It can repeat this process several times, and, every time the breaker closes, it causes another surge of current through the breaker, the transformer, and the lines, causing serious stress on the equipment. If you could tell immediately from the power waveforms that it was going to be a permanent fault, you wouldn't do the reclose cycling. Other power scenarios may play out over weeks or months.

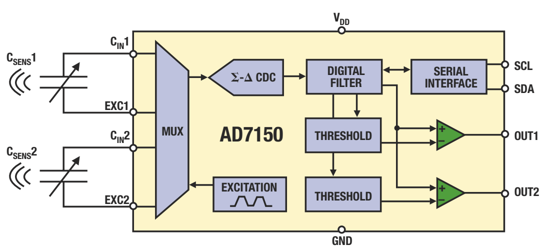
Awareness of the power performance all begins with the number crunching of digital-signal processing. Digital-signal processing is at the very heart of the intelligent grid, and advanced signal understanding via analytics transforms signal data into information that can be acted upon both by automated systems and by people. Ultimately, the intelligent grid allows the utility to measure and maintain power quality and reliability, perform sophisticated grid control, maximize asset utilization, and respond quickly—and, in many cases, automatically—to grid problems.—**by Margery Conner**

Providing an Edge in Capacitive Sensor Applications

The number of capacitance-based sensor designs in industrial, automotive, medical, and consumer applications is rising rapidly. Designers are continuously searching for new ways to use capacitive sensor technology to give their products an edge in a crowded marketplace. The trend is already in evidence where simple devices offering low to medium sensitivity are no longer sufficient to supply the demands of embedded sensor applications. Thick molding compounds, noisy environments, reliability concerns, and long interconnect distances from the sensor to the IC are just some of the new challenges facing capacitance sensor applications.

Robust Solution for Harsh Environments

Leveraging ADI's established capacitance technology, our AD7150 capacitance-to-digital converter delivers a robust signal processing solution for proximity sensing.

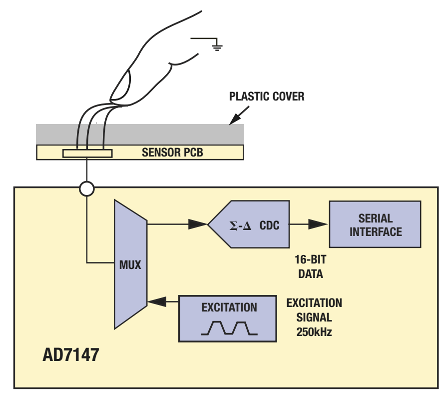


Capacitance-to-digital converter for proximity sensing.

This device offers automotive qualification, electromagnetic compatibility, adaptive environmental calibration, low power consumption, and a fast response time. Because of the AD7150's superior high sensitivity, capacitance sensors can be embedded deep inside thick molding compounds and still successfully perform the sensing function without compromising specifications. With a current consumption of 100 μA and a response time of 10 ms for both channels, the AD7150 enables low power, high speed capacitance sensor systems.

Noise Resilient, Space Saving

Answering the call for high resolution navigation, space optimization, and noise resilience in consumer devices, the AD7147 is the latest device in Analog Devices' CapTouch™ portfolio. This device raises performance for touch interfaces, boasting a three-fold improvement in sensor response over its predecessors and simplifying sensor design with a new single-electrode library. The active shield feature eliminates capacitance-to-ground pickup on board and provides shielding from other noise sources in the applications. This feature is unique to the Analog Devices solution and allows the sensor to be located remotely from the IC, without any compromise in the sensor response.



Capacitance-to-digital converter for touch control.

Implementing capacitance sensors requires a shift in focus from digital solutions to analog solutions. Capacitance-to-digital converters eliminate barriers to the advancement of portable and battery powered products by providing highly robust, sensitive solutions for use in a wide range of applications.

For more than 40 years, Analog Devices has solved "hard to do" problems in precision analog signal processing. Converting capacitance sensor signals is no exception. For more information about Analog Devices' capacitance sensing solutions, visit *www.analog.com/LI-CDC.* ▶

Author profiles: ***Conor Power*** *is a product marketing manager for instrumentation and automotive converter products at Analog Devices.* ***Garry O'Neill*** *is a product marketing manager for consumer input devices at Analog Devices.*

BY BONNIE BAKER

Outputs don't swing rail to rail

Single-supply amplifiers do not truly swing rail to rail at the output. Near the rail, the amplifier is nonlinear. For linear operation, the output of single-supply amplifiers can come within only 50 to 300 mV of each rail (**Figure 1**). Single-supply-amplifier, rail-to-rail-output ads can give a false sense of security. **Figure 1** shows a typical single-supply amplifier's output swing as you drive the output to the rails. The amplifier's linearity starts to degrade long before reaching the output-swing maximums, and the amplifier output never reaches either rail.

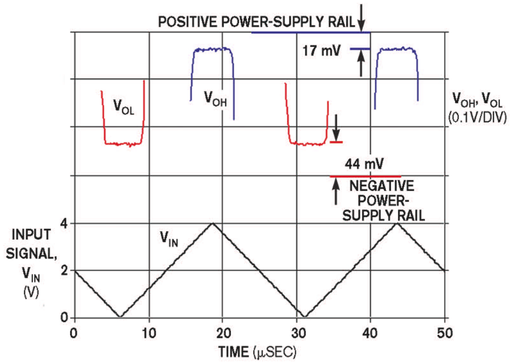


Figure 1 The lower plot illustrates the amplifier's input-voltage swing at a gain of 2V/V. The upper plot shows the amplifier's magnified output voltage.

The conditions of the dc-open-loop-gain specification define the amplifier's linear operating output range. The dc open loop gain in decibels is 20 $\log(\Delta V_{OUT}/\Delta V_{OS})$, where V_{OUT} is the output voltage and V_{OS} is the input offset voltage. When you drive the output high, V_H is the maximum voltage level at the output in the dc-open-loop-gain measurement. V_{OH} is the absolute maximum voltage level with respect to V_{DD} (drain-to-drain voltage) that the output can reach. V_L is the minimum voltage level at the output in the dc-open-loop-gain measurement, and V_{OL} is the absolute minimum voltage level that the output can reach. V_H is less than V_{OH}, and V_L is greater than V_{OL}.

From a signal-chain perspective, you can see an op amp's output limitations to swinging rail to rail when the op amp is driving an ADC. The FFT plot in **Figure 2a** shows the amplifier/ADC-combination response to a 1-kHz signal in a 5V system. The amplifier's typical closed-loop bandwidth is about 3 MHz with a typical slew rate of 2.3V/μsec. The amplifier output voltage swings from 140 mV to 4.66V. In this 5V-supply system, the headroom between the signal and rails is 140 mV. For this amplifier, the V_{OL} minimum specification is 15 mV above ground. The V_{OH} maximum specification is $V_{DD}-20$ mV.

Figure 2a illustrates the nonlinearity-output-stage effects with a single-supply CMOS amplifier by showing distortion at 2, 3, and 4 kHz and so on. By reducing the amplifier's output signal to 272 mV from each rail, the data looks perfect with only the ADC distortion (**Figure 2b**).

When using a single-supply amplifier, read the fine print! Some single-supply amps have output-stage charge pumps, allowing the amplifier's output swing to go to and well beyond the power-supply rails. In every case, read your data sheet and refer to the conditions on the open-loop-gain test. **EDN**

Bonnie Baker is a senior applications engineer at Texas Instruments. You can reach her at bonnie@ti.com.

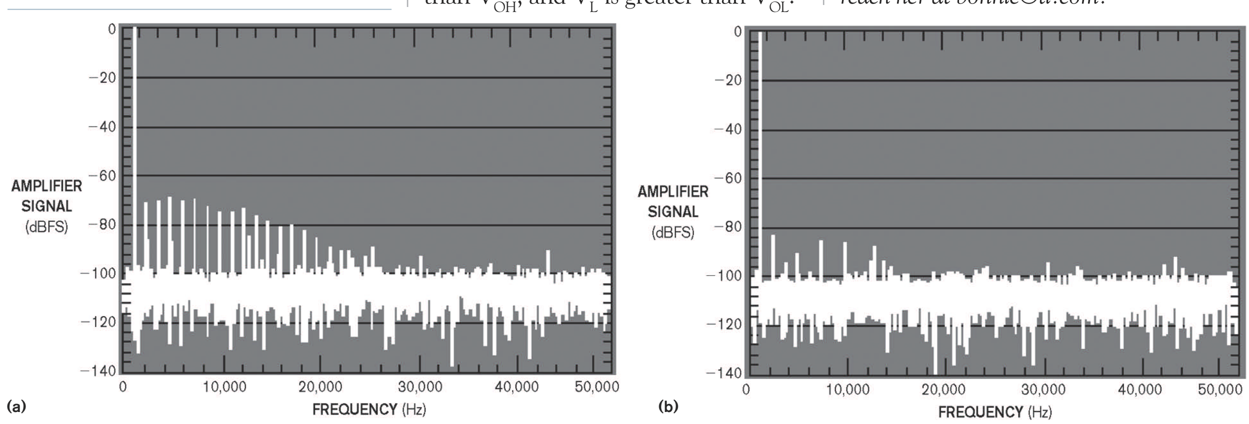


Figure 2 This 12-bit successive-approximation-register converter's maximum sampling speed is 100k samples/sec (a). Reducing the amp's output signal to 272 mV produces better results (b).

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+ Visit www.edn.com/070903pry for more in-depth coverage of the iPhone, including internal photography of various subsystems and useful links for additional research.

Apple's iPhone delivers more than just a dial tone

By now, you're probably overwhelmed with hands-on analyses of the iPhone, which Apple and partner AT&T began selling on June 29. Few reviewers, though, have cracked open the device's case and peered inside. Read on for details on the system building blocks that enable the iPhone to work its multifunction magic.

A 2M-pixel Micron CMOS sensor combines with a three-element, fixed-focus and -focal-length lens to create the iPhone's flash-deficient and still-image-capture-only camera.

The 3.5-in.-diagonal, 2×3-in. LTPS TFT (low-temperature-polysilicon-thin film-transistor) LCD delivers a 480×320-pixel, half-VGA resolution at 160 dpi, but Apple doesn't specify the display's native or dithered color depth. The touchscreen elements arranged in a coordinate system can support both self- and mutual-capacitance modes, thereby enabling simultaneous multitouch support; a Broadcom controller and an NXP Semiconductor ARM7TDMI manage the touchscreen.

The iPhone's RF board is jam-packed with ICs concentrated on one side of the PCB. Chips include an Infineon GSM/EDGE RF transceiver and companion Skyworks power amplifier and Epcos transmitter/receiver duplexer; a Marvell Wi-Fi transceiver and companion power amplifier from an unknown manufacturer; a Cambridge Silicon Radio Bluetooth transceiver; an Infineon cellular-baseband processor; and an Intel-labeled, single-package, two-die memory stack containing NOR-flash memory and pseudo SRAM—that is, self-refreshing, low-power DRAM with an SRAM-like system interface.

The main board assembly, swathed in EMI-shielding material, is a two-PCB digital/RF sandwich. One side of the digital board contains an STMicroelectronics accelerometer, a Wolfson Microelectronics audio codec, Linear Technology and NXP power-management ICs, a National Semiconductor MPL transmitter, a Texas Instruments LCD-boost converter, and a triumvirate of Samsung Semiconductor ICs: a 4- or an 8-Mbyte NAND-flash chip, depending on the iPhone model; 128 Mbytes of low-power, single-chip DDR SDRAM; and an ARM11 applications processor. The SIM connector dominates the digital board's other side, but it also houses a diminutive, 1-Mbyte SST flash memory, which probably acts as the ARM CPU's boot device.

A single flex circuit encompasses all of the iPhone's antennas: a combined Bluetooth/Wi-Fi element and a separate and much larger multiband cellular element. The planar antennas attach to the phone speaker's acoustical chamber.

The 3.7V lithium-ion battery consumes a dominant percentage of the iPhone's total volume and is a key determinant of the device's substantial specified battery life. Apple estimates that, after 400 recharge cycles, the battery will still retain 80% of its original capacity; replacing it will cost you $79 plus $6.95 shipping.

“A predictable supply of power, protected
from faults, is an essential ingredient of an efficient,
sustainable, manufacturing process.”

The 802.11n standard: GROWN UP AT LAST

THE 802.11N WI-FI STANDARD PROMISES MUCH. AFTER AN ESPECIALLY ANGST-RIDDEN DEVELOPMENT PROCESS, IT'S READY TO GO TO WORK.

BY ANN R THRYFT • CONTRIBUTING TECHNICAL EDITOR

Even for a wireless-communications standard, the 802.11n specification has over the last several years been subject to an exceptionally messy development process. Battling vendors and standards proposals, predraft and postdraft 1.0 silicon and box products, and multiple interoperability issues have continued to plague this latest generation of Wi-Fi technology. The 802.11n spec is now mostly past the difficult stage and about to fulfill its promise: a range approximately twice as great and transmitting speeds five to 10 times as fast as those of legacy 802.11a/b/g products (**Table 1**). It's about time, too, because the spec has a big job to do in designs for consumer, enterprise, campus, and metroscale markets. Unfortunately, the spec is complex and has a huge number of possible variants and options.

Those complexities are at least one reason that the process has taken so long. According to some industry participants, vendor infighting has been another major reason that the approval process has taken so long. Even before the IEEE committee approved Draft 1.0, at least three vendors had offered different proposals for the standard's core technology. TGn (Task Group N), the IEEE group that handles the spec, eventually narrowed down these competing proposals to two, says Jagdish Rebello, director and principal analyst of wireless communications for iSuppli. "Last year, [the two proposals] merged, and TGn submitted a joint proposal to the full body in May 2006." But TGn failed to achieve the necessary 75% approval level for a Draft 1.0 version. In March 2007, the committee voted to approve Draft 2.0, which came with approximately 3000 technical and editorial comments. Industry participants expect TGn to issue Draft 3.0 for a recirculation ballot this month, when the group expects to have completed the comment resolutions. As is usual for an IEEE standard, the specification will likely go through some more tweaking for another six to 12 months or so. The unprecedented number of options in this 802.11x spec makes this fine-tuning especially necessary, but participants agree that the mandatory sections are unlikely to change now.

During this lengthy, drawn-out process, at least one vendor coalition arose to develop an alternative specification so that products could more quickly get to market than the standards committee's work would support. In frustration at the length of time involved, manufacturers began releasing products even before Draft 1.0, based on different vendors' silicon designs. As tested by various external labs and research companies, many of these designs did not interoperate with each other.

To help push forward the standards-development process and provide interoperability certification, the WFA (Wi-Fi Alliance) in August 2006 announced that, during the first half of 2007, it would launch an extensive certification process for products that included baseline features from the developing standard. In May 2007, after TGn approved Draft 2.0, the WFA unveiled the Certified for 802.11n Draft 2.0 program, which it based on the mandatory sections of Draft 2.0, and announced the

first certified chip, card, and box products, which form the testbed for certifying additional products. The formal certification program began in June 2007. Many vendors have stated that their WFA-certified 802.11n Draft 2.0 products will be firmware-upgradable to the final IEEE 802.11n standard.

Netgear, whose products have now passed WFA certification, in 2005 launched Draft n products that it based on chips from two suppliers. "At that point, interoperability across chip vendors was an issue, and we had to supply two lines of adapters," says Som Pal Choudhury, Netgear's product-line manager for advanced wireless. The company's latest router product automatically detects and self-installs the most recent firmware from the company's Web site.

802.11N ADVANTAGES

The 802.11n WLAN (wireless-local-area-network) technology is the only Wi-Fi technology today with the bandwidth to support multiple HDTV (high-definition-TV) streams at 20 Mbps each. This performance is sufficient for implementing some long-standing goals of Wi-Fi networks. One of these goals, wireless multimedia, comprises voice/VOIP (voice over Internet Protocol), data, video, and gaming in residential applications. Another goal is achieving throughput, QOS (quality-of-service), and security levels that compare favorably with those of Ethernet which are necessary for enterprise-grade, campus, and municipal networks. But the methods of achieving this performance are complex, leading to many of the options and variants in the standard. Another main reason for all the options is the large number of device types that users want to connect to Wi-Fi networks, each with its own distinct set of requirements. Because the market for Wi-Fi has become much more heterogeneous than it was in the early days of 802.11x, 802.11n networks must accommodate a much wider range of device types; many of the standard's optional-requirement portions reflect that range. New requirements from consumer-electronics companies, such as video applications, or from the handset market, in which manufacturers are interested in power savings and better coverage, have contributed to the long, drawn-out IEEE process, as well as to the standard's complications, says Frank Hanzlik, managing director of the WFA. "There are a lot more people to please, so the compromise process has been more complex," he says.

But now that WLAN capability has penetrated the consumer and communications-device markets and is increasingly embedded into DSL (digital-subscriber-line) and cable modems, as well as into Apple TV, the markets are bigger, and the stakes are much higher, increasing motivation and helping to drive resolution of those conflicts. As a result, 802.11n Draft 2.0 has turned into more of a framework than a standard, says Craig Mathias, principal of the Farpoint Group. How difficult it will be for engineers to navigate that framework remains to be seen.

AT A GLANCE

- The IEEE's Task Group N has approved 802.11n Draft 2.0, the latest Wi-Fi standard, which promises approximately twice the range and five to 10 times the transmitting speeds of legacy 802.11a/b/g. Mandatory features probably won't change when the group issues Draft 3.0 for recirculation this month.
- Because of the large number of options possible under the standard—including RF band, channel width, number of antennas, and modulation scheme—not to mention additional options for specific device types, designing 802.11n products and determining their interoperability can be tricky.
- The Wi-Fi Alliance has begun interoperability testing of products under its Certified for 802.11n Draft 2.0 program, based on the mandatory features of Draft 2.0.
- Many vendors have said that their WFA-certified 802.11n Draft 2.0 products will be firmware-upgradable to the final IEEE 802.11n standard.

WHAT'S IN THE STANDARD?

The fact that products based on 802.11n can operate in either the 2.4- or the 5-GHz bands or both makes them potentially backward-compatible with legacy products. When you use 802.11n in the 2.4-GHz band and in a 20-MHz channel,it is backward-compatible either with 802.11b, using CCK (complementary-code-keying) modulation or with 802.11g, using OFDM (orthogonal-frequency-division-muliplexing) modulation. When you use 802.11n at 20- or 40-MHz channel widths in the 5-GHz band with OFDM modulation, it is backward-compatible with 802.11a. Devices built to conform to more recent 802.11x standards tend to employ OFDM because it is more efficient than CCK, which older Wi-Fi networks use. With 802.11g, OFDM has become the Wi-Fi-modulation scheme of choice. The 802.11n standard introduces more efficient OFDM modulation to increase data rate. It uses 52 data subcarriers instead of the 48 in legacy networks, producing 65 Mbps per spatial stream instead of the 54 Mbps of legacy 802.11a or g. Another option in the standard shortens the guard interval from 800 to 400 nsec to increase the OFDM symbol rate, further boosting the data rate.

Previous 802.11x standards specified only one frequency band, one channel width, one spatial stream—transmitting or receiving—per direction, and one maximum data rate. Aside from OFDM improvements to enhance throughput, the 802.11n spec also doubles the channel width and introduces frame aggregation, block acknowledgment, and spatial multiplexing; spatial multiplexing is one of several possible MIMO (multiple-input/multiple-output) configurations (see **sidebar** "What MIMO does"). It allows one or two channel widths, 20, 40, or both 20 and 40 MHz; one to four spatial streams in either direction; and at least two other MIMO options (**Table 2**). Transmitting-data rate for 802.11n networks is therefore highly variable and is based primarily on modulation scheme, channel width, and the number of spatial streams.

Depending on the design, an 802.11n-compliant product can reach a typical throughput of 144 Mbps, assuming OFDM modulation, two transmitting and two receiving streams—known as a 2×2 configuration—a 20-MHz channel width, or a—currently theoretical—maximum throughput of 600 Mbps, assuming OFDM modulation, a 4×4 configuration, and a 40-MHz channel width. Most 802.11n products operating today achieve transmitting speeds between these two extremes: 300 Mbps with OFDM, a 2×2 configuration, and a

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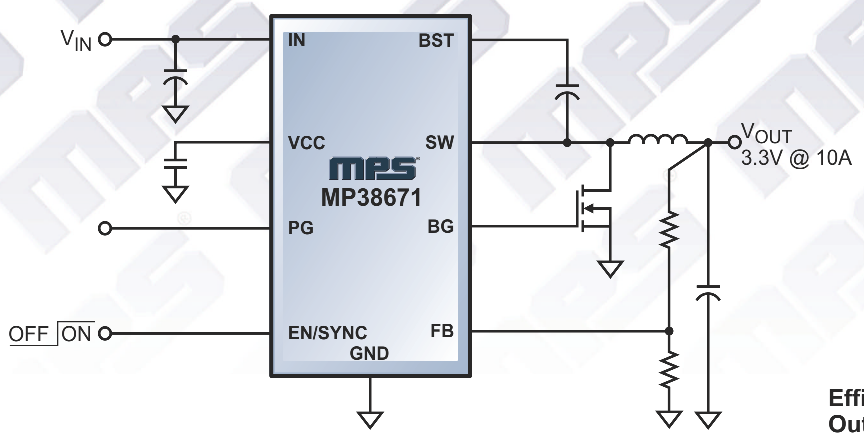

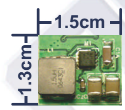

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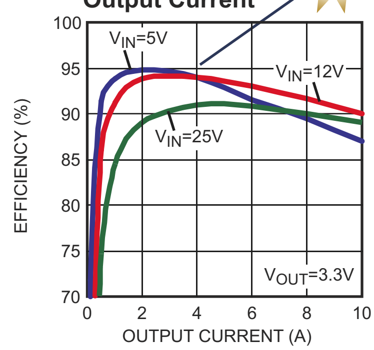

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MP38891	420KHz	4.5 - 30	0.8 - 15	6	
MP38874	600KHz	4.5 - 21	0.8 - 15	8	QFN 14
MP38671	600KHz	4.5 - 28	0.8 - 15	10	(3mm x 4mm)

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40-MHz channel width, or 450 Mbps by simply changing the MIMO configuration to 3×3.

As always, range also depends on several variables. But, with 802.11n, it's also more complex because of all the possibilities, including the transmitting power, number of receiving antennas, modulation scheme, and error-correction scheme. The spec also allows operation in 2.4- or 5-GHz frequency bands or a third dual-band 2.4/5-GHz option.

The differences between Draft 1.0 and Draft 2.0 are fairly minor, according to Bill McFarland, Atheros' chief technology officer and a member of the TGn. The biggest areas of change are associated with the coexistence mechanisms that govern how 802.11n devices behave with 802.11g devices, especially in the 2.4-GHz band. This issue is less important for 802.11a devices in the 5-GHz band: There, coexistence is simpler because the band is less crowded,

WHAT MIMO DOES

You can define MIMO (multiple-input/multiple-output) air-interface-technology methods in more than one way. The 802.11n Draft 2.0 spec includes spatial (space-division) multiplexing as the mandatory method for implementing MIMO and space-time block coding and beam forming as two optional methods. All of these methods use multiple antennas at both the transmitter and the receiver to send multiple data streams, increasing transmission speed, range, robustness, or some combination of these features without increasing bandwidth. These methods take advantage of the multipath effects, or reflections, inherent in RF communications. These reflections usually result in signal distortion at the receiver which, in turn, degrades performance.

In spatial multiplexing, which is mandatory in 802.11n, two to four antennas, each carrying a transmitting/receiving stream, simultaneously transmit multiple bits in the same frequency channel to increase throughput (Figure A). Because spatial-multiplexing techniques make receivers much more complex, designers usually combine them with OFDM (orthogonal-frequency-division-multiplexing)-modulation schemes, which are more efficient than other modulation schemes. Space-time block coding, an 802.11n option, uses different antennas for redundancy to increase robustness. The other optional method is beam forming, which uses multiple antennas as if they were parts of an array, forming a directional antenna that directs a beam to increase range.

The 802.11n spec allows one to four data streams for either the transmitting or receiving directions, but MIMO requires a minimum of two for each direction. In applications in which higher data rates, accurate data reception, and longer distances are critical, such as when incorporating 802.11n into a residential gateway, designers might want to increase data streams to three receiving and three transmitting for maximum data throughput. Further, they should use the best coding schemes, says Jagdish Rebello, director and principal analyst of wireless communications for iSuppli. "But if you're looking at a consumer product, such as a handset, you can fall back to the lowest configuration possible, such as single input, multiple outputs." Most applications use a two-transmitter/two-receiver (2×2) configuration, which is the minimum configuration that the Wi-Fi Alliance's Certified for 802.11n Draft 2.0 certification program is testing.

Access-point devices usually need symmetrical data streams. Asymmetrical arrangements, with more receivers than transmitters, improve receiver performance by way of better data correlation and range, which are especially useful in client devices, such as laptops and handsets. Because each antenna adds a radio chain, power consumption and cost of the silicon increase in both the RF and the baseband portions.

"This [cost and power-consumption issue] has historically been a challenge," says Broadcom's Kevin Mukai, senior product-line manager for 802.11n products. "That's where CMOS integration comes in. We've been pushing down the power budget to get 802.11n functionality onto smaller form factors." The advantages of a 2×2 configuration in silicon, such as Broadcom's chip set, are fewer antennas and therefore lower cost. The 802.11n spec incorporates a mandatory power-save mode for handsets. As single-chip silicon for 802.11n begins to appear, perhaps within the next year, greater opportunities for scaling down power will emerge.

"The cost, power consumption, and size of 802.11n silicon are issues that we, as an industry, still need to work through," says Craig Mathias, principal of the Farpoint Group. "But we're good at that."

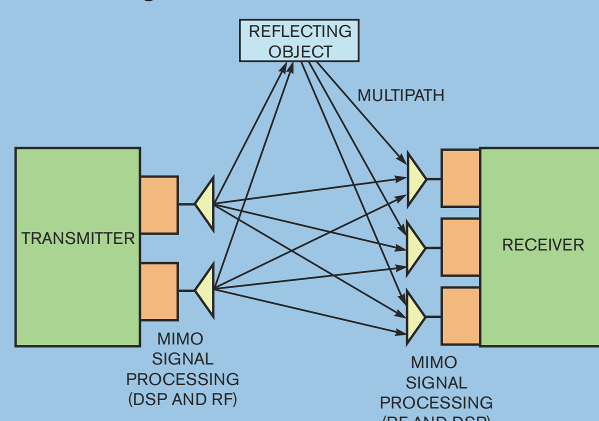

Figure A MIMO methods transmit multiple data streams to increase transmission speed, robustness, range, or some combination of these features (courtesy Farpoint Group).

TABLE 1 802.11N DRAFT 2.0 AND 802.11G COMPARISON

Feature	802.11g	802.11n Draft 2.0	Comments
RF band	2.4 GHz	2.4 GHz, 5 GHz	802.11n devices can be either single- or dual-band (2.4/5-GHz)-capable.
Channel width	20 MHz	20 MHz, 40 MHz	802.11n accommodates 20 MHz, 40 MHz, or both 20 and 40 MHz.
No. of transmitting or receiving spatial streams	One	One, two, three, or four	Common 802.11n transmitting and receiving configurations include 2×2, 2×3, 3×3, 3×4, and 4×4, but any combination of one to four streams per direction is possible.
Modulation schemes	Mostly OFDM; also backward-compatible with CCK and DSSS	Mostly OFDM; also backward-compatible with CCK and DSSS	OFDM encodes more bits per symbol than CCK based on the density of the QAM mode (maximum 64 points).
Typical transmitting data rate	25 Mbps with OFDM	144 Mbps with OFDM, 2×2, 20-MHz channel width	802.11n data rate depends on channel width, number of spatial streams, and modulation scheme.
Maximum transmitting data rate	54 Mbps with OFDM	600 Mbps with OFDM, 4×4, 40-MHz channel width	Current 802.11n equipment can transmit 300 Mbps with OFDM, 2×2, 40-MHz channel width, or 450 Mbps with OFDM, 3×3, 40-MHz channel width.
Typical indoor range	30 to 35m	50 to 70m	Range depends on multiple variables, including transmitter power, number of receiver antennas, modulation schemes, and error-correction schemes.
Typical outdoor range	110m	160m	Range depends on multiple variables, including transmitter power, number of receiver antennas, modulation schemes, and error-correction schemes.
802.11x backward compatibility	802.11b: 2.4-GHz band, CCK or DSSS, 20-MHz channel width	802.11b/g when you use 802.11n at a 20-MHz channel width in the 2.4-GHz band, CCK/OFDM (b/g); 802.11a when you use 802.11n at a 20- or 40-MHz channel width in the 5-GHz band, OFDM	802.11b maximum data rate is 11 Mbps. 802.11a maximum data rate is 54 Mbps.

Sources: Atheros, Broadcom, iSuppli, and Wi-Fi Alliance.

Notes: CCK=complementary-code keying. DSSS=direct-sequence spread spectrum. OFDM=orthogonal frequency-division multiplexing. QAM=quadrature-amplitude modulation.
2×2 denotes a two-transmitter/two-receiver configuration. 2×3 denotes a two-transmitter/three-receiver configuration. 3×3 denotes a three-transmitter/three-receiver configuration. 3×4 denotes a three-transmitter/four-receiver configuration. 4×4 denotes a four-transmitter/four-receiver configuration.

and most devices perform OFDM-style transmission and exceptions. Also, the layout and organization of the frequency channels work well with 802.11n. "In contrast, the 2.4-GHz band includes 802.11b devices using CCK modulation, and the frequency channels are laid out in a way that doesn't match up as well with how 802.11n likes to use the frequency," he says.

It's also difficult to get 802.11n devices to work well together with 802.11b and other devices in the 2.4-GHz band when using 40-MHz channels that double the data rate, because of potential interference issues. Techniques for dealing with this problem are still under discussion, and Draft 3.0 will probably resolve them, says McFarland. Some of these techniques are high-level-politeness algorithms based on measuring the amount of traffic in the environment: If there's a lot of traffic, channel width remains at 20 MHz. If traffic is low, channel width can expand to 40 MHz to take advantage of greater bandwidth. Another possible method calls for actively "listening" to detect any nearby access points or networks and moving to 20-MHz mode if any are detected, regardless of the amount of traffic. TGn is discussing modifications of this variant because it's potentially problematic.

Other, more fine-grained methods for preventing interference, such as CCA (clear-channel assessment), operate on a packet-by-packet basis. To prevent collision, before a 40-MHz-wide packet is transmitted, CCA checks to make sure that both channels are clear and that the packet can be transmitted on that whole 40-MHz frequency range. This option will probably remain. The spec now requires the use of both high-level-politeness and more fine-grained mechanisms. How the high-level algorithm will work is under discussion.

"At the MAC [media-access-control] layer, the concern is how devices share the airwaves on a packet-by-packet ba-

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TABLE 2 MAJOR 802.11N DRAFT 2.0 MANDATORY AND OPTIONAL FEATURES

802.11n Draft 2.0 specification feature type	802.11n Draft 2.0 specification feature	Tested by Wi-Fi Alliance Certified for 802.11n Draft 2.0 program	Explanation	Comments
Mandatory	MIMO spatial multiplexing	Support for two spatial streams in transmitting mode, two spatial streams in receiving mode (2×2); mandatory for Wi-Fi Alliance certification.	Transmitting mode required for access-point device, receiving mode required for access-point and client device, except for handheld devices	Simultaneously transmits multiple bits from different antennas, increases throughput
Optional	MIMO space-time block coding	Not tested	IEEE still finalizing details; candidate for future certification program	Uses different antennas for redundancy and increases robustness; targets handheld devices
Optional	MIMO beam forming	Not tested	IEEE still finalizing details; candidate for future certification program	Uses multiple antennas as an array to form a directional beam, increases range
Mandatory	Aggregated MAC Service/Protocol Data Units	Support for both; mandatory for Wi-Fi Alliance certification	Required for all devices	Improves MAC-layer efficiency by increasing maximum frame size (frame aggregation)
Mandatory	Block ACK	Support for block ACK; mandatory for Wi-Fi Alliance certification	Required for all devices	Improves protocol efficiency and throughput by reducing size of block-ACK frame and enabling back-to-back frame transmissions
Optional	2.4-GHz operation	Single-band device in 2.4-GHz band; tested if implemented	Devices must operate in one of three modes: single-band, 2.4-GHz; single-band, 5-GHz; or dual-band, 2.4- and 5-GHz.	802.11n devices can be either single- or dual-band (2.4/5-GHz)-capable. Most current 802.11n devices use 2.4-GHz band.
Optional	5-GHz operation	Single-band device in 5-GHz band; tested if implemented	Devices must operate in one of three modes: single-band, 2.4-GHz; single-band, 5-GHz; or dual-band, 2.4- and 5-GHz.	NA
Optional	Dual-band 2.4- and 5-GHz operation	Access-point or client-device capable of supporting both 2.4- and 5-GHz bands; tested if implemented	Devices must operate in one of three modes: single-band, 2.4-GHz; single-band, 5-GHz; or dual-band, 2.4- and 5-GHz.	NA
Mandatory	20-MHz channel width	Tested at 2.4 or 5 GHz for both one and two spatial streams	NA	802.11n accommodates 20 MHz, 40 MHz, or both 20 and 40 MHz.
Optional	40-MHz channel width	Tested only in 5-GHz band, if implemented, for one and two spatial streams; 40-MHz operation poses interference risks in crowded 2.4-GHz band.	IEEE has not yet decided protocol for allowing 40-MHz operation in the 2.4-GHz band.	Doubling legacy 20-MHz channel width can double throughput.
Mandatory	Mixed-mode operation: 802.11n with a, and 802.11n with b/g	Tested in both access-point and client devices	Mixed mode with b/g is mandatory for all 802.11n devices operating in the 2.4-GHz band; mixed mode with 802.11a is mandatory for all 802.11n devices operating in the 5-GHz band.	NA
Optional	Greenfield-mode operation: 802.11n only	Tested in both access-point and client devices if implemented	NA	Improves efficiency by eliminating support of legacy devices in an all-802.11n network
Mandatory	Protection protocols	Tested in both access-point and client devices	Mandatory when legacy networks and devices are within range. IEEE is discussing other optional methods.	Prevent negative impact on legacy-device traffic by 802.11n transmissions
Optional	Power-save multipoll	Not tested	NA	Saves handset power consumption in time-slotted network when 20 or more VOIP handsets connect to a single access point
Not in spec	NA	Optional untested features must not disrupt Wi-Fi Alliance-certified features and expected functions.	Required for all devices	NA

Sources: Atheros, Broadcom, iSuppli, and Wi-Fi Alliance.

Notes: ACK=acknowledgment. MAC=media-access control. MIMO=multiple input/multiple output. VOIP=voice over Internet Protocol.

sis," says McFarland. "The biggest enhancement here in Draft 2.0 versus 1.0 is packet aggregation." Traditionally, in 802.11x, a packet is transmitted and retried until an acknowledgment is returned. In 802.11n, mandatory packet aggregation combines a large number of packets into one superframe, sends it, and gets back a block acknowledgment specifying which packets were and were not received correctly. Only packets that failed must be retransmitted, resulting in a more efficient system and making better use of the high data rate. Additional differences in Draft 3.0 are likely to include changes to some of the spec's optional modes and features, including MIMO methods.

When a product implements one of the spec's optional features, the 802.11n spec provides for a negotiation associated with that feature so both devices can determine which options they include, says McFarland. But complications may arise in network configurations. For example, if the network requires beam forming, currently optional, both access points and clients must support it. Clients without that feature can still interoperate, but the network doesn't have the resulting performance enhancement.

For the first phase of its Certified for 802.11n Draft 2.0 program, the WFA defined a set of features that corresponds closely to most of the mandatory features of 802.11n Draft 2.0. The program also tests some of the spec's optional features if the device under test implements them.

In its second phase, currently targeting summer 2008, the program will test some optional features that the IEEE is considering for inclusion in the spec. The WFA has not yet decided how to label these capabilities. One possibility is a profile concept, or sets of features that correspond to the requirements of classes of devices, such as one set for PCs and data-centric devices; another for consumer devices that require video and audio streaming; and another that might include handheld devices requiring voice, VOIP, and telephony features. "This [arrangement] would give us better combinations of mandatory and optional features that make sense for that usage class," says the WFA's Hanzlik.

Available 802.11n chip sets differ in whether they target use in access points or client equipment and enterprise or consumer devices. They also have performance differences and varying MIMO configurations. Chip sets for 802.11n consist of CMOS baseband MAC engines, a separate CMOS radio, and an external discrete power amp.

Single-chip 802.11n silicon will likely become available within the next year or so. Legacy Wi-Fi a/b/g single-chip silicon already exists in CMOS SOCs (systems on chip), says Kevin Mukai, Broadcom's senior product-line manager for 802.11n products. Single-chip silicon will be more of a challenge for 802.11n products, because the a/b/g SOCs contain only one RF chain per chip, but 802.11n requires multiple RF chains. **EDN**

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AUTHOR'S BIOGRAPHY

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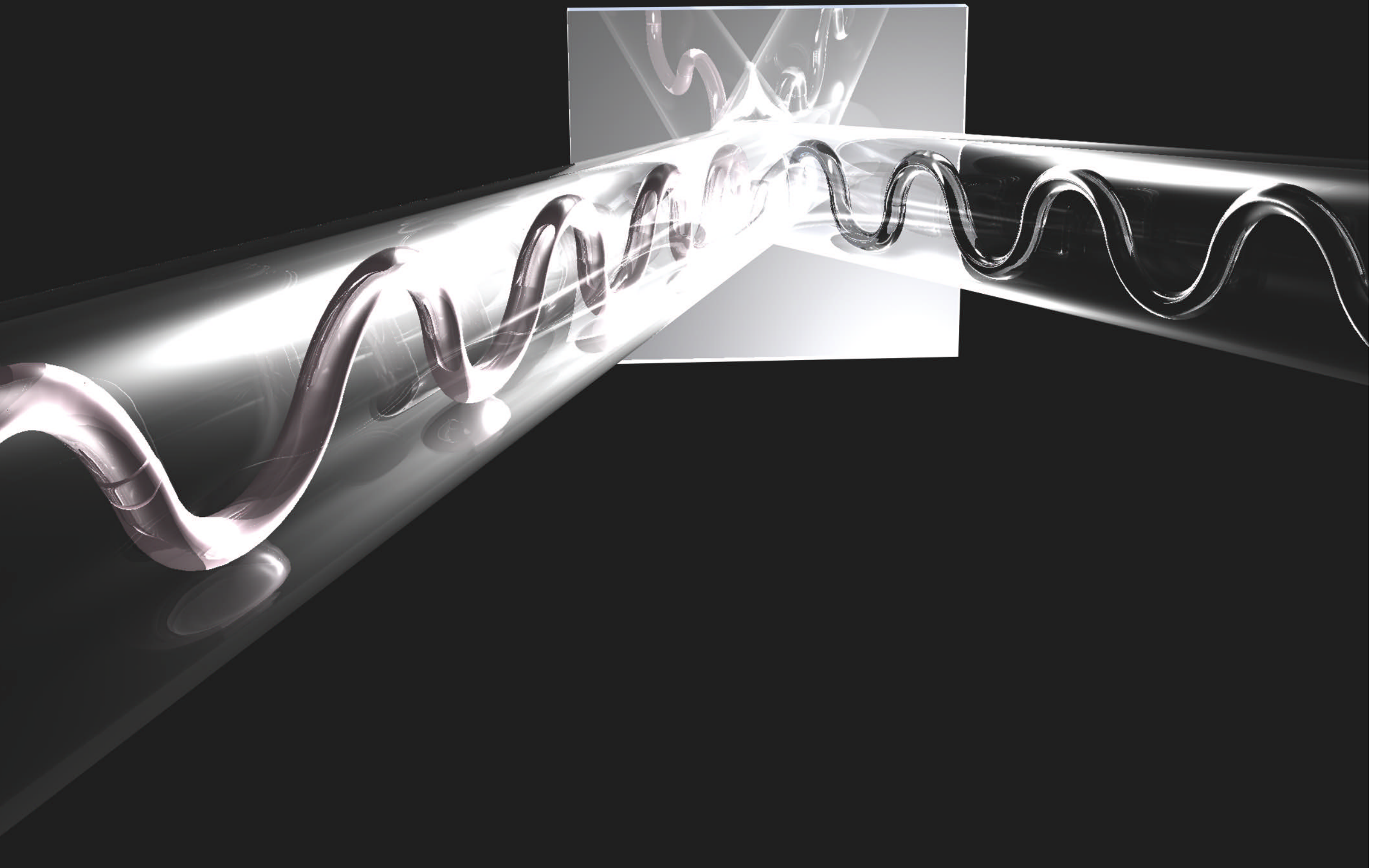
TDR: taking the pulse of signal integrity

BY PAUL RAKO • TECHNICAL EDITOR



TIME-DOMAIN REFLECTOMETRY WILL HELP YOU DESIGN AND TROUBLESHOOT CABLES, CONNECTORS, FAST PCB TRACES, AND HIGH-SPEED PACKAGES. WITH TDR INSTRUMENTS, YOU CAN ENSURE THE SIGNAL INTEGRITY OF FAST DIGITAL SIGNALS AS THEY TRAVEL ACROSS YOUR SYSTEM. BOTH ANALOG AND DIGITAL ENGINEERS NEED TO UNDERSTAND AND USE THESE TECHNIQUES.

TDR (time-domain-reflectometry) measurements can provide a direct representation of the signal integrity of a cable or PCB (printed-circuit-board) trace and can analyze ICs' performance and failure. A TDR setup sends a fast pulse down the cable or PCB trace and displays the returning reflections, which indicate changes in impedance. The impedance changes can be radical, such as an open or a short, or they can be as subtle as the few femtofarads that a PCB via adds. The technique, in the form of OTDR (optical TDR), takes advantage of the equivalence between dielectric constants in electronic systems and the index of refraction in optical systems.

HISTORY OF TDR

Engineers in the late 1930s began taking TDR measurements to measure dielectric constant and moisture content in soils. Engineers today still use the technique to evaluate many geophysical measurements, such as earthquake faults and bridge "scour," a hazardous condition that occurs during times of rapid river flow and especially under icy conditions. Currents transporting sediments away from bridge piers, buried utilities, and similar structures cause this condition (**references 1**, **2**, and **3**). After World War II, engineers performed TDR testing with separate pulse generators and oscilloscopes. Digital-logic chips generated pulses with 5V swing—more than enough amplitude to create reflections large enough to detect. A major advance occurred in the late 1960s when Hewlett-Packard (now Agilent) introduced the 1415A plug-in instrument for its 140 mainframe scope. This high-performance instrument was the first to integrate the pulse generator and sampling head into one unit. In the 1970s, Tektronix announced the 1502 and 1503 TDR-test sets, which found wide use in testing cable integrity. The military was an avid user of TDR equipment, and Tek offered military-specification versions of these products. Nuclear-bomb testing needed TDR to evaluate the miles of cables going "down hole" as well as to evaluate geophysical phenomena in the blasting area.

The technical achievements of Tektronix and HP would continue through the coming decades. HP developed the 20-GHz 54120A mainframe and 54121A test head (**Figure 1**). These products consisted of the first computerized-TDR-test set and performed TDT (time-domain transmission), which required another input to monitor the transmission of the circuit in addition to the input that sends the pulse and digitizes the reflection. This approach allows characterization of the losses experienced through the circuit; you cannot measure these losses with a purely reflective instrument. The scope used the detector from an HP network analyzer in its sampling head.

By the 1980s, Tektronix had introduced the 50-GHz 11801 scope mainframe and the 20-GHz SD-24 differential TDR module (**Figure 2**). By monitoring the transmission with another module, the 11801 could perform TDR and TDT and could evaluate differential signals, such as those in LVDS (low-voltage-differential-signaling) and SCSI (small-computer-system-interface) circuits. The scope evolved to the 11801C, whereas the module, with a 35-psec-rise-time pulse generator, remained unchanged. This scope was for many years the workhorse of the industry, despite its somewhat arcane user interface, perhaps more suited to operation through GPIB (general-purpose-interface-bus) control than for use by an engineer using the front panel. HP did not rest on its laurels, soon thereafter introducing the 18-GHz 54754A module for the 86100A mainframe. Tektronix followed with the 17-psec 80E04 module for the CSA803, which it derived from the 11801C. Current Tek models include the 70-GHz DSA8200 mainframe and the 50-GHz 80E10 modules. Competitor LeCroy, meanwhile, offers the 100-GHz Wave-Expert 100H with a 20-GHz ST-20 TDR module (**Figure 3**).

Picosecond Pulse Labs makes what is perhaps the ultimate TDR: The 4022 add-on module accepts the pulse from a Tek, an Agilent, or another TDR and speeds it to an astonishing 9-psec rise time. Picosecond also makes pulse generators, but making the 4022 speed a pulse that a scope launches has advan-

tages. "We did it that way so it would work with the existing software in the scopes," says Clayton Smith, Picosecond's chief technology officer. Picosecond also makes the TDR modules for various scope OEMs.

In addition to this high-end evolution of TDR, several instruments have evolved to do what TDR started out doing in the 1950s: examine long cables for shorts, opens, and breaks. This function was important to the US Navy because modern warships have miles of cables. Frustrated radio and TV broadcasters also have used TDR to find nicks in the coaxial cable on antenna towers, the results of youngsters' using the towers for target practice. The Tektronix TS90 TelScout TS90 100 is one such machine; another, the Spirent model E2520 tester, can evaluate twisted-pair-cable runs as long as 9800 feet.

PREMISE OF A TECHNIQUE

The theory of TDR involves some mathematics relating to wave propagation and transmission-line impedance (**references 4** and **5**). The physical phenomena of TDR are far more accessible and intuitive. It seems normal that a wave bounces off a short or an open section of cable. Most of you have directly observed this phenomenon. Slightly more challenging is the notion that a wave propagating into an open circuit adds to the incoming wave, doubling it, whereas a wave propagating into a dead short reflects back the negative potential, bringing the incident wave to 0V. As you would expect, if the transmission line is terminated in its characteristic impedance—50Ω for a 50Ω cable—then no reflection occurs, and the pulse remains unscathed. It is only logical that a terminating resistor with a value a bit higher than matching causes a slight bump in the pulse reflection and that a resistor with a slightly lower value causes a dip in the pulse. The reflection cases for terminations that are inductive or capacitive are also intuitive, because a capacitor is a short at high frequencies, and an inductor is an open at high frequencies (**Figure 4**).

AT A GLANCE

- TDR plots provide a representation of impedance over distance.
- Modern high-speed instruments can resolve distances of millimeters.
- You can use software to convert TDR (time-domain-reflectometry) data to S parameters.
- You can create SPICE models from TDR data.
- Sampling scopes can provide wide bandwidths at relatively low cost.

The classic lumped-element model of a transmission line yields another handy fact: That model is a string of inductors with interstitial capacitors shunting to ground. The ratio between the capacitance and the inductance determines the exact value of the characteristic impedance—50, 75, or 300Ω, for instance. Physics demonstrates that a wire in space has inductance, because, whenever a current flows through that wire, the current creates a field that must satisfy Gauss' Law: If the volume within an arbitrary closed mathematical surface holds a net electric charge, Q, then the electric flux, Φ, through its surface is Q/ϵ_0.

Think of a wire in space as providing the distributed inductance that you see in a lumped-element model of a transmission line. Now, imagine bringing that wire in space close to a ground or reference plane. This proximity provides the lumped capacitance of the model. It seems that bringing the wire closer to the plane should lower the impedance, because the capacitance has increased. Similarly, a wide spot over a ground plane in a PCB trace also increases capacitance and decreases the impedance along the spot. A via acts as a small capacitor, coupling to the plane and lowering the impedance. Conversely, a small jumper wire, such as that in a connector finger, rises off the board and away from the ground plane, thus lowering the distributed capacitance and increasing impedance along that section of the transmission line. With a TDR setup, you can touch your finger or a metal tool to the PCB trace and watch the resultant impedance change—as you add capacitance—directly on the scope screen.

The theory of TDR states that the faster the pulse rise time, the smaller the features the instrument can resolve. The simple cable testers of the past had rise times of nanoseconds. Today's TDR instruments, however, can examine short cable and PCB-trace runs, connector impedance, and IC-package impedance. As such, they require rise times on the order of 10 to 30 psec. These fast pulses require a fast scope to record the reflections and transmissions. The extreme speed requirements for high-reso-

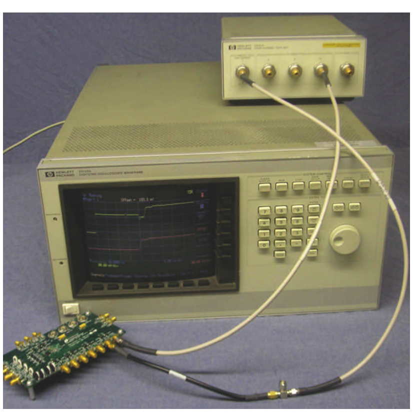


Figure 1 The HP 54120A mainframe, in concert with the 54121A test head, can take single-ended TDR and TDT measurements.

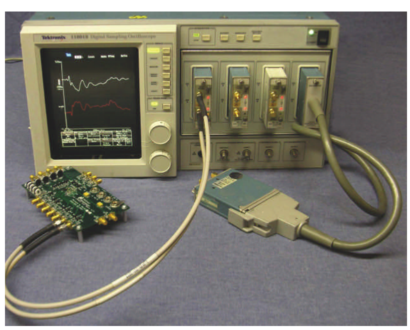


Figure 2 This Tektronix 11801B with four SD-24 TDR modules can take four pairs of differential TDR measurements. The scope traces show 10Ω of variance on PCB traces that should be 50Ω. The TDR shows how to improve this situation with layout and connector selection.

Figure 3 You can equip LeCroy's top-of-the-line sampling scope, the WaveExpert 100H, with ST-20 TDR modules.

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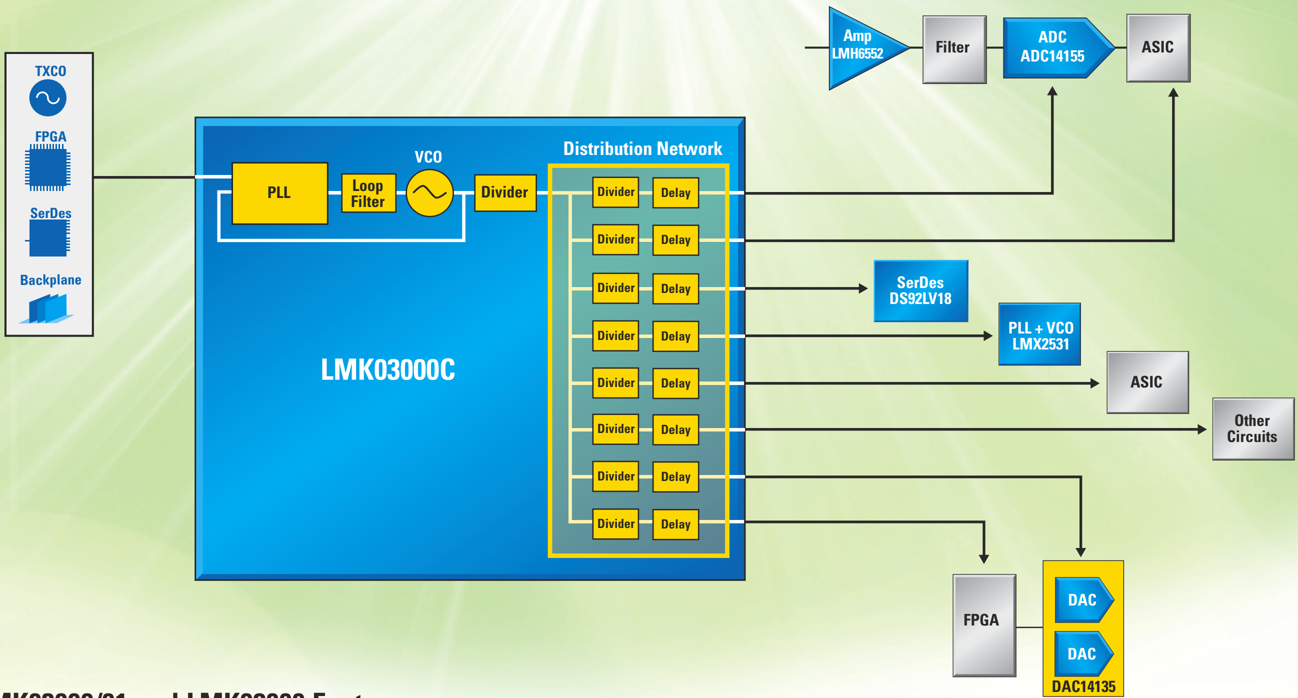

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LMK03000C/LMK03001C	400 fs
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lution TDR measurements dictate that TDR modules almost always are parts of sampling, or "equivalent-time," oscilloscopes, with relatively low sample rates. Fast analog amplifiers in the front end of these units support bandwidth that is far higher than that of the best real-time

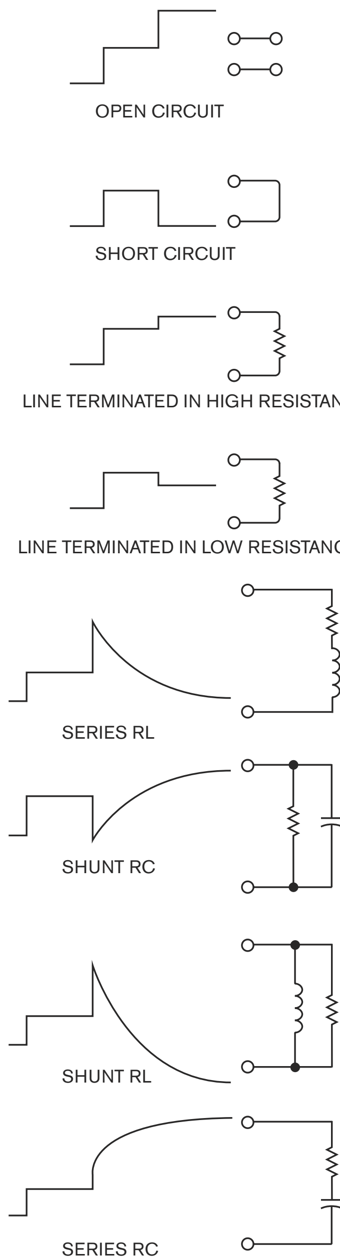

Figure 4 The reflections from various terminations or transmission-line variations reveal the nature of the impedance along the line and at its termination. The transmission line can be a long cable or the bond wire inside an IC.

scopes. The trigger circuit in the scope slightly shifts the unit's acquisition points after each trigger event (**Figure 5**). This technique "paints" the fast wave as one set of slew samples appears on the screen for each trigger event. Sampling scopes work only with repetitive waveforms, however. A video, radar, or cell-phone signal that differs on every sweep would display as just a blur. This limitation is not a problem with TDR testing because the pulses are repetitive waveforms that you can continuously launch into the test circuit, giving the sampling scope time to build the waveform.

"Originally, sampling scopes were developed to address the bandwidth needs that couldn't be addressed with real-time scopes," says frequent *EDN* contributor and Tektronix Product Marketing Manager Dima Smolyansky, whose article, "TDR and S-parameter measurements: How much performance do you need?" appears on pg 61 of this issue. "Real-time scopes are in the 10- to 20-GHz domain, but sampling scopes can still get you to wider bandwidths—70 GHz and beyond. … A sampling scope is more accurate in the time domain, but, even better, for the same bandwidth, it is a low-cost solution compared to a real-time scope."

DESIGN CONCERNS

System-level engineers feel more comfortable in the time domain than in the frequency domain that RF and analog-IC designers favor. System-level engineers see TDR as a more natural and intuitive way to explore the performance of high-speed circuits. In contrast, the frequency-domain equivalent to TDR is scattering, or S, parameters. One elegant body of theory depicts the equivalence of the information in either measurement technique (**Reference 6**). You can measure S parameters directly in the frequency domain with a VNA (vector-network analyzer), which sweeps a sine wave of fixed amplitude into a circuit while recording the amplitude and phase of the reflections and transmitted signal. Knowing the phase and amplitudes of these S parameters allows you to characterize the circuit for as wide a frequency band as the oscillator in the VNA can sweep. VNAs have a wide dynamic, or SNR (signal-to-noise-ratio), range and

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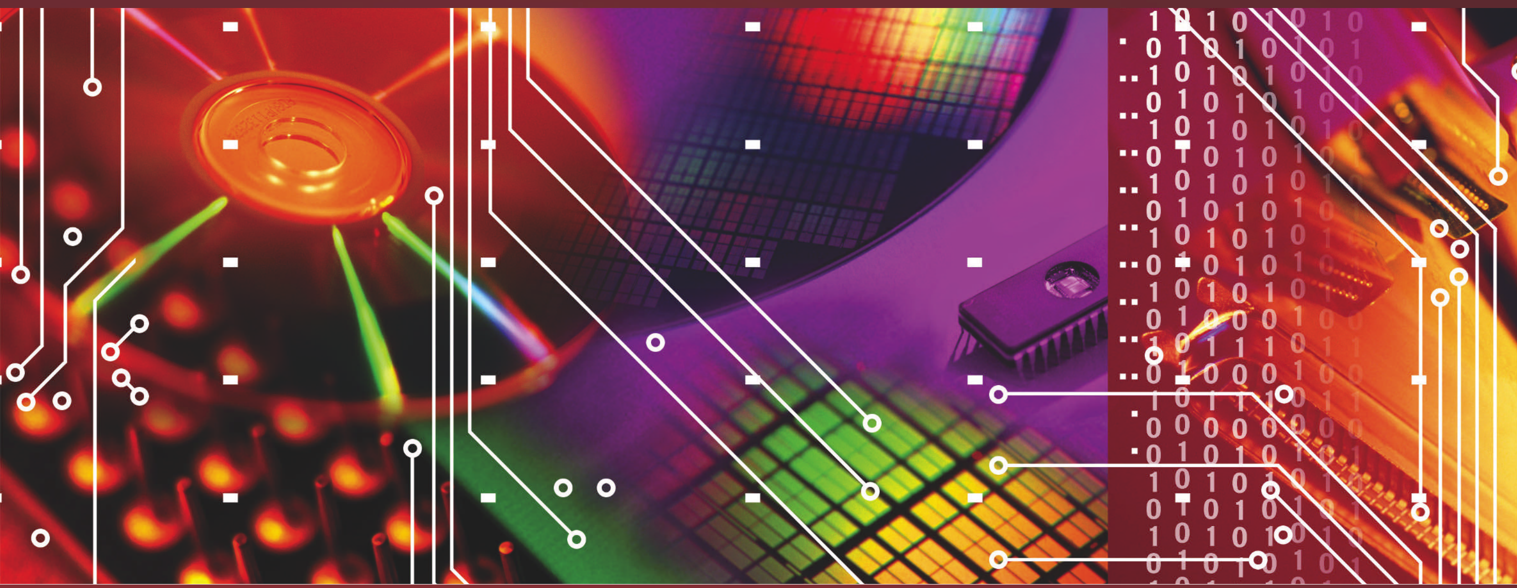

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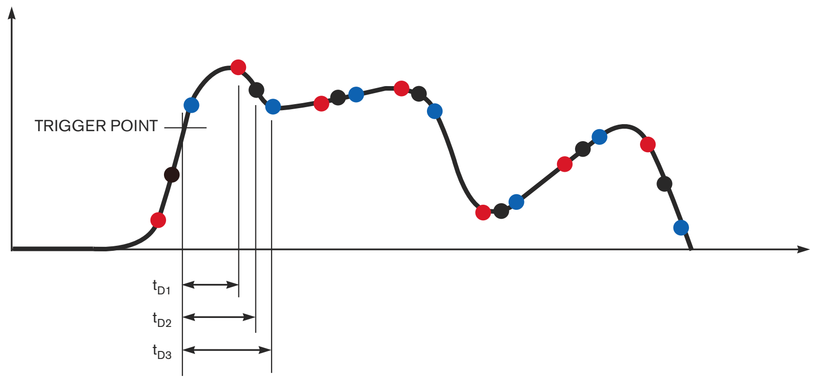

Figure 5 A sampling, or equivalent-time, oscilloscope does not take all the points in a single sweep. It varies the delay from the trigger to the acquisitions to build up a representation of the waveform over many repeated sweeps by adding a small set of points to the waveform each sweep. It first takes the red points; adds to the delay; and then adds the black points, the blue points, and so on. Because the scope is acquiring constantly, it also provides a pretrigger acquisition.

narrow-bandpass filters that sweep in concert with the oscillator; thus, they reject most of the out-of-band noise. In contrast, you must take TDR measurements using a wideband oscilloscope, so it has the higher rms-noise floors that all wideband circuits exhibit.

RF and microwave engineers prefer S parameters over VNAs for good reasons; one reason is their dynamic range, which can approach 130 dB. In addition, RF engineers often need to know the steady-state behavior of the circuit. They assume that the oscillators in their circuit are running and that a fairly narrow frequency band—say, the 1900-MHz cell-phone frequency—is passing through the system. Engineers who worry about signal integrity, on the other hand, must worry about the entire frequency spectrum. They may need to know how their system will react to a string of pulses after a dc voltage has been on the cable or trace. This situation makes it even more preferable to use TDR measurement. Engineers designing PLLs (phase-locked loops) have both problems: They must characterize the operation of the loop once it is running, and they also have the time-domain problem of having to watch the loop lock in after milliseconds or more. This problem might represent millions or billions of cycles of the dominant operating frequency of interest and makes PLL development especially challenging. These issues make the design, simulation, and testing of PLLs daunting tasks (**Reference 7**).

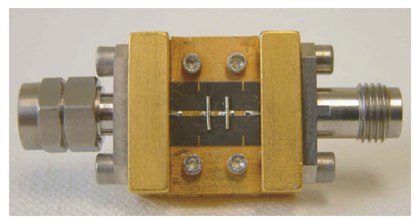

Figure 6 This test fixture has two small wires soldered across the transmission line connecting the two connectors. These wires add capacitance and show up as reduced impedance on a TDR plot (courtesy Picosecond Pulse Labs).

Engineers should heed some warnings despite the mathematical equivalence of S parameters in the frequency domain and TDR in the time domain. The FFTs (fast Fourier transforms) and inverse FFTs that exist between the time and the frequency domains are important calculations, often involving causality and passivity (**Reference 8**). A causality problem occurs when the calculation does not account for transit time and other delays leading to time-domain issues. A similar problem occurs with passivity: The inverse transform into the time domain may impart energy in passive-circuit elements, producing erroneous results. Going from the time domain to the frequency domain also imposes SNR limitations. Because the time-domain measurement suffers from broadband noise, even the best TDR setups produce only 50-dB SNR at high frequencies. This figure may be adequate. Alternatively, you may need to take the

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List Price (500 channels)	**$13,915** Uses 8 of 8 slots	$32,257 Uses 18 of 18 slots
	Features	
I/O to computer	Industry Standard LAN, USB, GPIB	Proprietary PCIe-MXI
Scanning speed	109 chan/sec	140 chan/sec
Size	3U vertical space in rack	4U vertical space in rack
Front panel	Yes	No
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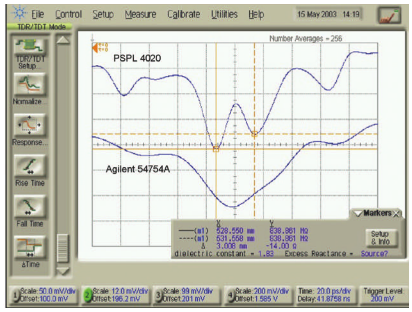

Figure 7 The two small wires in Figure 6 cause these dips in impedance. Using a 9-sec pulse generator causes the top trace, and the scope's internal pulse generator causes the bottom trace (courtesy Picosecond Pulse Labs).

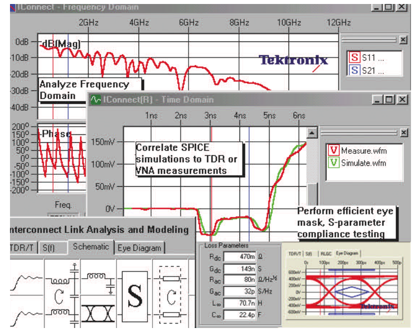

Figure 8 Tektronix offers iConnect software that can convert TDR data to S parameters and can create SPICE models from the data.

S-parameter data directly in the frequency domain with a VNA. Remember to balance the convenience of being able to take S parameters and TDR measurements on one machine with the need to verify at least one measurement in both domains. Still, some TDR setups perform correlation with a 9-psec-rise-time TDR and a 50-GHz VNA, so you can convert between domains if you properly use the appropriate equipment (**Reference 9**). Reliable S-parameter data from a TDR setup requires a pulse generator with short rise times and an oscilloscope with wide bandwidth. Similarly, generating TDR data by taking an inverse FFT of S-parameter data requires adequate bandwidth on the VNA to give the detail you wish to see in the time domain.

You can achieve impressive spatial resolution with a good TDR setup (**figures 6** and **7**). The advent of faster-than-10-psec pulse generators and 50- or 100-GHz-bandwidth scopes allows the use of TDR in IC-package development and failure analysis. If the TDR setup can resolve impedance over millimeters, then you can see the effects of bond wires and whether metallization damage is causing an IC to behave unexpectedly. With a fast pulse generator and scope, you can achieve small spatial resolutions (**Table 1**). In addition, some high-performance scopes incorporate software techniques that further improve the effective resolution by calibrating out reflections from fixtures and cables leading to the circuit or device under test.

Eliminating the effects of the test fixture is only one of the benefits of modern TDR-scope software. The Agilent 86100A mainframe's software allows you to take differential-TDR measurements with two positive pulses. Using pulses of the same polarity on both channels ensures that the same waveform excites both channels. It is difficult to make the rise time and fall time of a pulse exactly opposite, so differential-pulse generation introduces a common-mode error. The Agilent scope

TABLE 1 SPATIAL RESOLUTION OF TDR MEASUREMENTS

Rise time (psec)	Dielectric				
	Air (microns, ϵ_R=1)	Teflon (microns, ϵ_R=2.1)	FR4 (microns, ϵ_R=4.6)	Alumina (microns, ϵ_R=9.8)	Gallium arsenide (microns, ϵ_R=12.9)
5	750	518	350	240	209
10	1500	1035	699	479	418
15	2250	1553	1049	719	626
40	6000	4140	2798	1917	1671

Courtesy Picosecond Pulse Labs

sends two pulses of the same polarity; its software then inverts and applies superposition to the response, so that the resultant waveform is identical to—but has less error than—that of a differential TDR. "The accuracy goes up because of the much better matching of the electronics," says Joachim Vobis, a product manager at Agilent.

LeCroy has similarly powerful software in its WaveExpert 100H scope. The standard TDR-analysis package can calibrate out the test fixture and generates two-port differential S parameters from the TDR data. The scope includes a wizard to guide the user through the setup and calibration procedure. You can also set the rise times of the internal pulse generators for 20 psec to lower values that serial-interface standards groups specify.

Inside Tektronix's DSA8200 sampling scope, software provides TDR and TDT as just one part of an entire package that analyzes communication parameters. Tek also offers iConnect software that can run on the DSA8200 mainframe or standalone on a PC (**Figure 8**). It converts TDR data to S parameters, analyzes jitter, and enhances the native TDR resolution of the DSA8200. The software also uses TDR data to deduce a SPICE model of the circuit under analysis, allowing you, for example, to create a SPICE model of a ribbon cable that carries LVDS serial data at high speeds. You can then give this SPICE model to IC designers to show the complex impedance of load or to evaluate the transmission medium in a system-level simulation.

TDR has gone from a simple technique used to check cables to a sophisticated method of performing complete time-domain characterization of fast digital signals. TDT has also evolved, achieving resolutions at which you can use it to examine and characterize the internal structures and circuits inside ICs. In addition, capable software has pushed the art of TDR from looking at bumps on a scope trace to calibrated results in ohms and inches. The software allows the TDR data to generate S-parameter frequency-domain characterizations and even deduce an equivalent SPICE model. The scope traces that generate the models can also verify any simulations with the models and produce valid results.

TDR results have one important advantage over frequency-domain analysis: A TDR plot shows the location of impedance problems in a circuit. "It helps you isolate problems that may show up with a VNA in the frequency domain, but you will not know where in the circuit the problem is," says Picosecond Pulse Labs' Smith. "The TDR shows you the exact spot in the signal path where the problem is occurring." Smith goes on to note some real-world issues with high-speed connectors: "We bought a whole slew of edge-launch SMA [Sub-Miniature Version A] connectors to evaluate with our test setups. We saw a huge difference in the signal integrity through these connectors. In one, it was obvious that the engineers used a VNA and frequency-domain analysis, but the TDR response was horrible." You would not want to use those connectors for fast digital data streams or any analog signal that had fast edges. With TDR, you get instant, intuitive results that show you where you can improve your circuits. Be sure to have this valuable measurement technique in your arsenal of troubleshooting skills. **EDN**

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TDR and S-parameter measurements: How much performance do you need?

TIME-DOMAIN TECHNIQUES ARE CHALLENGING ESTABLISHED FREQUENCY-DOMAIN MEASUREMENTS IN THE ANALYSIS OF HIGH-SPEED SERIAL NETWORKS. TO OBTAIN MEANINGFUL RESULTS, THE MEASUREMENT EQUIPMENT MUST HAVE ADEQUATE RISE TIME, BANDWIDTH, AND DYNAMIC RANGE. YOU CAN DERIVE THE INSTRUMENTATION REQUIREMENTS FROM THE NETWORK STANDARDS.

In computers, communications, and consumer electronics, the transition from parallel to high-speed serial-data transmission is creating new design challenges. Increasing data rates push more bits per unit time through the same interconnect link, entering the multigigabit-per-second regime and creating substantially tighter timing budgets. Because of high-frequency interconnect losses, higher data rates also exacerbate ISI (intersymbol interference). Moreover, to achieve still faster data transmission, many standards allow several serial links to operate in parallel, creating multilane configurations, in which crosstalk plays yet another important role.

As a result, you must more closely manage the characterization of interconnect reflections, losses, and crosstalk. You must also differentially perform this characterization, and do it in the frequency, rather than the time domain, using so-called S-parameters (see **sidebar**, "S-parameter backgrounder" at the Web version of this article at www.edn.com/ms4245). S-parameters provide quantitative insight into the causes of bit er-

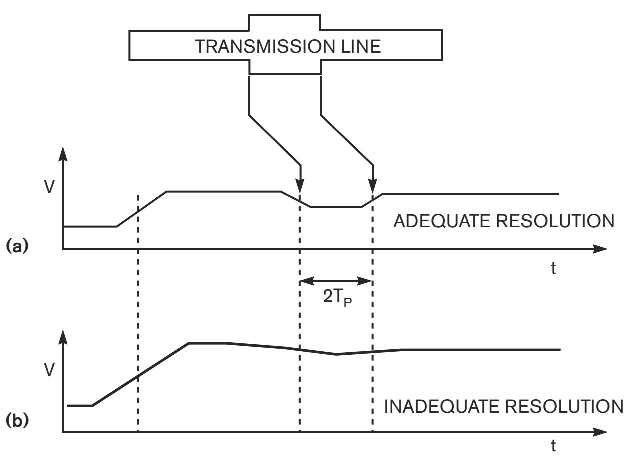


Figure 1 The IPC specification TM-650 summarizes the resolution and TDR rise-time requirements for typical surface microstrips in air (a) and on FR4 PCBs (b).

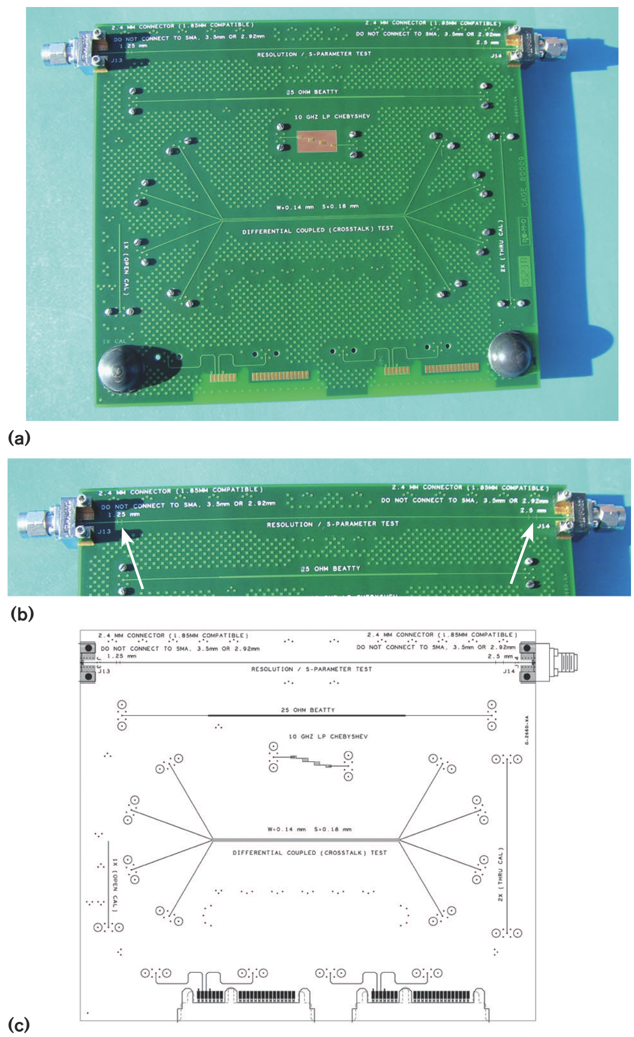
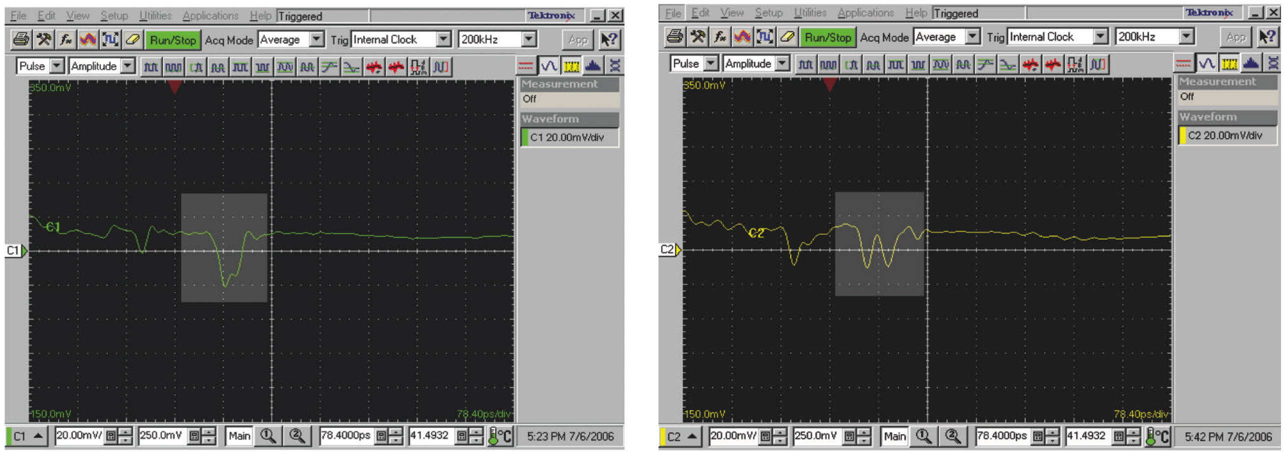


Figure 2 A typical TDR demo board (a and b) includes a resolution structure (c). The arrows highlight discontinuities created by two pairs of vertical bars—the left-hand pair separated by 1.25 mm; the right-hand pair, by 2.5 mm.



(a) (b)

Figure 3 TDR testing of the structure in Figure 2 uses a 15-psec reflected rise time, producing these results for 1.25-mm spacing between discontinuities (a) and 2.5-mm spacing (b).

rors, BER (bit-error-rate) degradation, jitter, ground bounce, and EMI (electromagnetic interference). You can also measure crosstalk by using S-parameters to characterize signal transfer among adjacent transmission-line pairs. Many electrical standards, such as SATA (Serial Advanced Technology Attachment), PCIe (Peripheral Component Interconnect Express), Fibre Channel, and 10GbE (10-Gbps Ethernet), now use S-parameters in their compliance-test procedures. The umbrella term "SDNA" (serial-data-network analysis) describes differential serial-data-compliance testing and differential characterization of serial-data components.

The traditional S-parameter-measurement tools are VNAs (vector-network analyzers). These instruments are powerful, but that power may well be their undoing, because they achieve their accuracy with the aid of extensive calibration procedures. For SDNA applications, these differential calibration procedures can be excruciatingly lengthy and difficult to follow, resulting in long test times and sensitivity to human error. Electronic calibration modules for VNAs are available, but they operate only at frequencies that are relatively low for most SDNA applications. Moreover, the cost of VNAs tends to be higher than that of the instruments that most digital designers have on their workbenches.

TDR (time-domain-reflectometry)-based S-parameter measurement tools have proved to be cost-effective, easy to calibrate and use, and accurate enough for SDNA (see **sidebar** "TDR-based S-parameter measurements" at the Web version of this article at www.edn.com/ms4245). They also provide higher throughput than VNAs. For example, by using TDR and postprocessing software, you can obtain a differential insertion-loss measurement within a minute instead of the 15 minutes or so a VNA can require. Moreover, VNAs can't measure directly to dc, and on long devices under test, such as cables, they can take a long time to accurately measure low frequencies. Most VNAs also compute systems' differential response from single-ended measurements because, until recently, more accurate direct-differential measurement was too difficult and expensive.

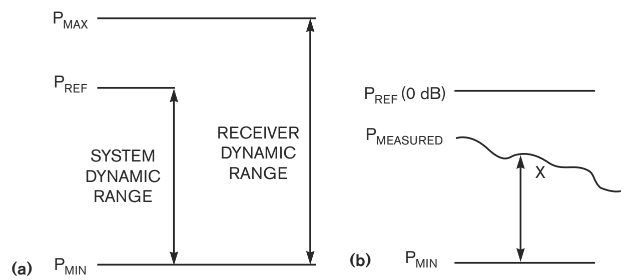


Figure 4 You typically define receiver dynamic range as the difference between the maximum and minimum measurable power—P_{MAX} and P_{MIN} (a)—and system dynamic range as the difference between the source's nominal power (P_{REF}) and the minimum measurable power (P_{MIN}) (b).

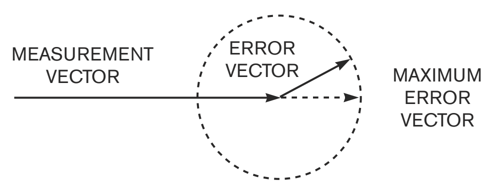


Figure 5 The diameter of the error circle represents the total peak-to-peak ripple.

TDR-based systems can directly measure dc and low frequencies. For example, by simultaneously firing multiple sources, Tektronix's (www.textronix.com) DSA8200 and IConnect S-parameter-measurement system can directly obtain true-differential TDR and S-parameters. IConnect also allows the acquisition of records as long as 1 million points, a requirement for S-parameter measurements on long devices, such as cables. Finally, the typical cost of a TDR-based system can be as little as half that of a VNA system that makes comparable SDNA measurements, and the TDR system provides higher time-domain resolution than does a VNA with comparable bandwidth. Several misunderstandings exist about TDR-based S-

parameter measurements (see **sidebar** "Misconceptions about TDR-based S-parameter measurements" at the Web version of this article at www.edn.com/ms4245). Overall, TDR-based S-parameter-measurement systems provide an easy-to-use, high-throughput approach to performing S-parameter-compliance tests in accordance with many digital standards as well as tests used in characterizing digital devices that operate at gigabit-per-second speeds.

TDR SPATIAL-RESOLUTION REQUIREMENTS

Start with the most basic requirement for TDR: providing sufficient resolution for locating faults in a device package or on a PCB (printed-circuit board). The IPC (Institute for Printed Circuits) document TM-650 2.5.5.7a defines TDR resolution as "the resolution limit … wherein two discontinuities or changes on the transmission line … begin to merge together … According to this definition, the resolution limit is half the … 10 to 90% rise time or 90 to 10% fall time (depending on whether the TDR response is calibrated with a short or open circuit)" (**Reference 1**).

Using **Table 1**, which you can find at the Web version of this article at www.edn.com/ms4245, IPC TM-650 summarizes the resolution and TDR rise-time requirements for typical surface microstrips in air and on an FR4 PCB (**Figure 1**). (In FR4, propagation velocity of electromagnetic waves is approximately 2×10^8m/sec—approximately two-thirds that in free space.) A board's inner layer, or stripline, is more representative of a typical board run. In addition, it is useful to provide resolution data for propagation in air. For a stripline, assume a propagation of 0.446 times the propagation velocity of light in free space. **Table 2**, also at www.edn.com/ms4245, summarizes the resulting resolution data. Now look at a practical situation. On a typical TDR-demonstration board (**Figure 2**), the resolution structures are reasonably close to the board's 2.4-mm S connector (see **sidebar** "Precision microwave-connector care and compatibility," also at www.edn.com/ms4245).

Figure 3 presents the results of TDR testing with a 15-psec reflected-rise-time TDR module, with the signal launched from the left to access the 1.25-mm structure and the signal launched from the right to access the 2.5-mm structure. Clearly, on the structure with 2.5-mm separation, the two discontinuities have perfect resolution, whereas on the structure with 1.25-mm separation, you start to lose resolution. (The trace on the demo board is a microstrip, and, according to **Table 1**, there is a different limit on the resolution for microstrips.) The interesting question is, however: What happens for spacing shorter than 1.25 mm between discontinuities? The discontinuities do not disappear; they simply become one discontinuity. Clearly, then, when a failure analyst attempts to locate a single discontinuity, even a submillimeter discontinuity is observable with the TDR module. The following is an important conclusion: With 15-psec reflected rise time, an advanced module can achieve submillimeter resolution.

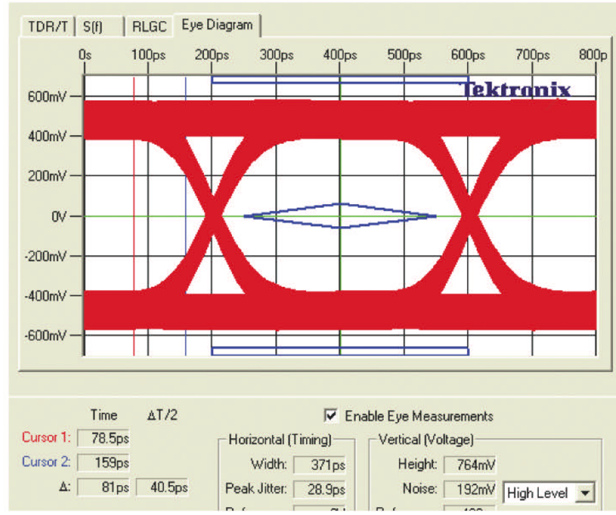


Figure 6 In this 2.5-Gbps signal, crosstalk causes eye closure that is 10% of the amplitude.

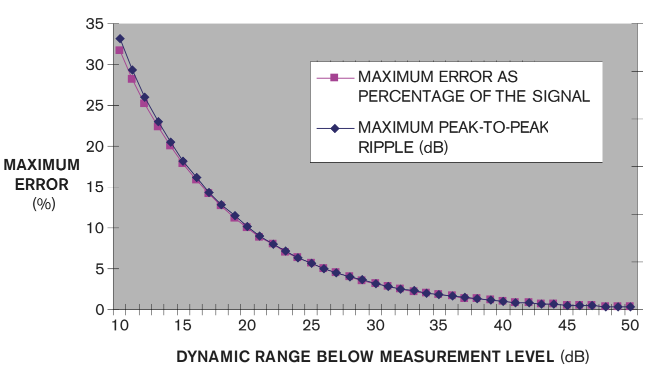


Figure 7 Increasing the dynamic-range requirement decreases the maximum allowable ripple and error.

RISE-TIME REQUIREMENTS

When using a TDR-based S-parameter measurement system for characterization or for a compliance test that a specific standard defines, it is important to know what the rise time must be to permit accurate measurements or testing. When specifying the rise time, standards focus primarily on the maximum, or slowest, rise time and look at the minimum rise time only as an informative parameter. SATA test procedures, for example, state the required minimum rise time, but then a footnote clarifies: "Failures at minimum rate have not been shown to affect interoperability and will not be included in determining pass/fail for interoperability testing" (**Reference 2**). So, for most standards, the question for a designer remains: What is the TDR rise time I need to test in accordance with the standard for compliance with a given specification, at a given data rate, with a given S-parameter bandwidth?

A recent study of standards revealed a clear trend in which rise times for first-generation standards, such as InfiniBand SDR (single data rate) and PCIe (Peripheral Component Interconnect Express), constituted a substantially smaller portion of the bit duration, or unit interval, than those of the second-generation standards, such as InfiniBand DDR (double

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data rate), PCIe 2.0, and 4-Gbps Fibre Channel, or third-generation standards, such as 8-Gbps Fibre Channel and 10GbE (gigabit Ethernet). You can draw an approximate dividing line between the generations of standards at 3.125 Gbps for the first- to second-generation transition and 6.5 Gbps for the second- to third-generation transition. The rise time constituted approximately 15% of the bit duration for the first-generation standards, 20% for the second generation, and 25% for the third generation. All rise times are 20 to 80% of the transition time (**Table 3** at www.edn.com/ms4245).

A designer who uses a TDR rise time that is 50% faster than the rise time of the devices in the controlling standard can achieve complete characterization of the channel with a more-than-adequate guardband. Note that TDR rise time is the time it takes a signal to traverse 10 to 90% of the transition range, which provides an additional guardband compared with the standards' 20 to 80% rise-time specification. This assumption ensures that the rise time is sufficiently fast for characterization. If you need to slow down the rise time, you can either mathematically filter the oscilloscope or use sufficiently lossy cables or filters. Using this 50% guardband assumption specifies how much TDR rise time several standards require.

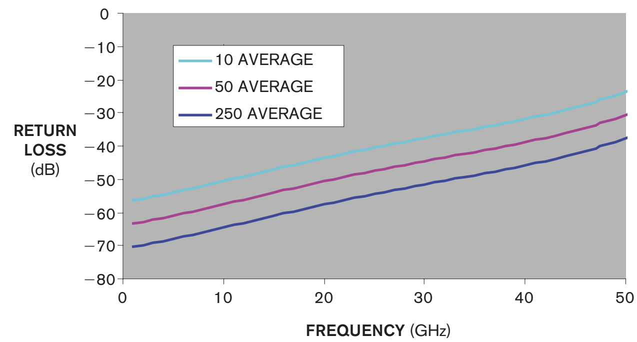

Figure 8 The dynamic range of a high-end TDR module depends slightly on what you are measuring, decreases with increasing frequency, and increases with the number of averaged signals.

DYNAMIC RANGE

Typically, receiver dynamic range is the difference between maximum and minimum measurable power—P_{MAX} and P_{MIN} (**Figure 4a**). System dynamic range is the difference between the nominal power of the source (P_{REF}) and the minimum measurable power (P_{MIN}, **Figure 4b**). In TDR-based S-parameter measurements, P_{MAX} relates to a sampling module's maximum operating specification and is less relevant when you focus on passive-component, or interconnect, measurements. As a consequence, system dynamic range matters for serial-data-interconnect characterization.

You may wonder how the definition of dynamic range relates to serial-data dynamic-range requirements. Dynamic range is, in essence, the difference between 0 dB and the noise


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floor. The accuracy of the measurement at a given frequency depends on the difference between a measurement level ($P_{MEASURED}$) and the noise floor (P_{MIN}). If your device under test has a measured noise floor of X dB below the measurement-reference level, you can show that the accuracy, or error, in percentage points relates to X dB below the reference value by the following **equation**:

$$\mathrm{ACCURACY} = 10^{\left(\frac{-X(dB)}{20}\right)}\%.$$

Note that, in the frequency domain, because the signal and noise add vectorially, the **equation** shows worst-case error when the noise vector is in phase or 180° out of phase with the signal vector. Additionally, you can show that the total peak-to-peak ripple, the error-circle diameter in **Figure 5**, on that signal is Y dB using the following **equation**: Y dB=20[log (100%+accuracy%)−log(100%−accuracy%)].

This **equation** includes both the positive and the negative ripple on the waveform. You can now show accuracy that you can achieve depending on how far the dynamic range is below the measurement level (see **Table** "Accuracy versus dynamic range below measurement level" at the Web version of this article at www.edn.com/ms4245). For a typical characterization in any of the serial-data standards, you would want to measure a voltage no smaller than approximately 10% of the full-signal amplitude. Such a voltage glitch can result from reflections or from crosstalk from an adjacent differential-line pair. A voltage glitch of this type still provides an 80% eye opening (**Figure 6**).

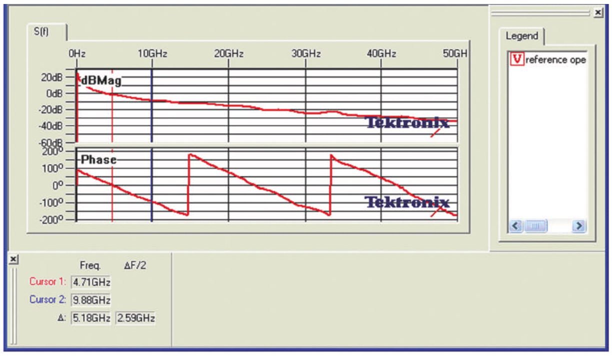

Figure 9 The TDR module is phase-linear, but its incident power declines with increasing frequency.

It is adequate to measure this voltage glitch with 10% accuracy, which translates into accuracy that is 1% of the full-signal amplitude). The minimum measured voltage size and accuracy requirements for 10%±1% at 0.5, 1V, and 2V signals are 50±5, 100±10, and 200±20 mV, respectively. Using the curves of **Figure 7**, you can determine that a signal that is 10% of the total amplitude is −20 dB. To measure this signal with

no more than 10% error, the noise floor must be another 20 dB below the measurement level, making the total dynamic-range requirement 40 dB.

FREQUENCY REQUIREMENTS

Later generation standards place less stringent requirements on characterization of digital components. In the first- and second-generation standards, designers talked about characterization to the clock's fifth harmonic, even though the standards required much less stringent compliance testing. In third-generation standards, designers talk about characterizing to the third harmonic. Overall, performing characterization to the fifth harmonic ensures adequate characterization bandwidth and provides designers with sufficient confidence. Using the fifth harmonic as a guideline, **Table 4** at www.edn.com/ms4245 provides the frequency requirements.

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Figures 8 and **9** present the dynamic range that TDR test equipment requires for SDNA applications. Notably, dynamic range degrades with frequency. The degradations result primarily from the steplike nature of the TDR-incident waveforms, which cause the incident power to roll off as 1/f. **Table 4** at www.edn.com/ms4245 shows how several standards relate to the dynamic-range and bandwidth requirements.

Based on expert user knowledge, this article identifies accuracy requirements for SDNA debugging, compliance, validation, and characterization and defines the requirements for SDNA applications. Those requirements are TDR rise time to resolve the smallest relevant discontinuity, TDR rise time for component characterization in accordance with various standards, and dynamic-range and bandwidth requirements for such characterization. **EDN**

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AUTHOR'S BIOGRAPHY

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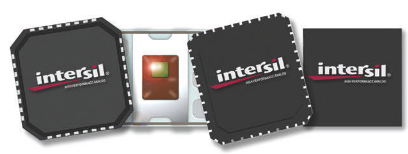

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FPGA-based design yields low-cost arbitrary-frequency generator

AN FPGA-BASED DESIGN IS PERFECT FOR PRODUCING AN ARBITRARY-FREQUENCY GENERATOR WITH BROAD APPLICATIONS IN BIOMEDICAL DEVICES AND ANYWHERE ELSE THAT YOU NEED SIGNALS OF HIGHLY ACCURATE, PRECISELY KNOWN FREQUENCY. THERE ARE SOME SUBTLETIES TO THE CIRCUIT'S OPERATION THAT YOU SHOULD KNOW ABOUT, THOUGH.

Many systems divide a crystal frequency by an integer number to generate clock signals. Unfortunately, the integer divisor limits the available set of output frequencies. Applications such as arbitrary-waveform and -frequency generators and biomedical-signal simulators require low-jitter signals at odd sets of frequencies. For such applications, you can use a phase-accumulator-based frequency generator.

Look at the math. Consider a sinusoidal waveform, which **Equation 1** describes:

$$Y = \sin(wt) = \sin(2\pi ft) = \sin(\Phi), \qquad (1)$$

where w is frequency in radians per second, f is the frequency in hertz, t is time, and Φ is the phase in radians.
As time increases by Δt, the phase increases by $\Delta\Phi$:

$$\Delta\Phi = 2\pi f \Delta t. \qquad (2)$$

From **Equation 2**, you can define the frequency as:

$$f = \frac{\Delta\Phi}{2\pi\Delta t}. \qquad (3)$$

In **Equation 3**, you can consider Δt to be a sample clock, or a clock period, which the crystal oscillator defines. Thus, the meaning of **Equation 3** is that, to produce frequency, the phase must increase by $\Delta\Phi$ radians with every sample-clock period.

You can express Δt in terms of the sampling-clock frequency:

$$\Delta t = \frac{1}{f_{CLK}}. \qquad (4)$$

By combining **equations 3** and **4**, you obtain the **equation** for the frequency:

$$f = \frac{\Delta\Phi f_{CLK}}{2\pi}. \qquad (5)$$

You can use **Equation 5** to generate an arbitrary frequency. To do it, you need a device that increases in phase by $\Delta\Phi$ radians with every clock period. You can implement such a device as a phase accumulator—a binary counter, which contains a value that increases by ΔN counts with each clock pulse.

A binary counter with k stages can generate 2^k numbers, corresponding to the full 2π-radian period. Similarly, you can replace the phase increase in radians, $\Delta\Phi$, by the phase increase in counts, ΔN. Switching from radians to counts produces:

$$f = \frac{\Delta N f_{CLK}}{2^k}. \qquad (6)$$

From **Equation 6**, to obtain frequency, you must increase the value in the phase accumulator by ΔN counts with every clock:

$$\Delta N = \frac{f 2^k}{f_{CLK}}. \qquad (7)$$

CIRCUIT IMPLEMENTATION

You can, for example, design a circuit that uses a 24-bit phase accumulator and a 20-MHz-input-crystal clock. Suppose you need to obtain an output frequency of 501.1 Hz.

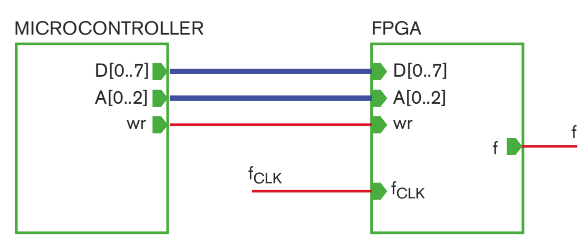

Figure 1 The microcontroller calculates ΔN from Equation 8 and clocks it into the FPGA using the 8-bit data bus, the 2-bit address bus, and the wr control signal.

From **Equation 7**, ΔN is:

$$\Delta N = \frac{501.1 \times 2^{24}}{20E6} = 420 \text{ COUNTS.} \quad (8)$$

With each input-clock pulse, the value in the 24-bit counter increases by 420 counts. When the counter rolls over from the maximum 2^k value, the counter generates an output-signal one-to-zero transition. Thus, you can use the phase accumulator's MSB (most-significant bit) as an output frequency.

Figure 1 shows an FPGA that connects to a microcontroller. The microcontroller calculates ΔN from **Equation 8** and clocks it into the FPGA using the 8-bit data bus, the 2-bit address bus, and the wr control signal. Because the phase accumulator's MSB is an output, you can represent ΔN in (k−1) bits. In other words, ΔN cannot exceed 2^{k-1}. The Verilog source code of **Listing 1** implements the FPGA functions. The following two numerical examples reveal how the circuit operates.

The first example requires an output frequency of exactly 10 MHz. From **Equation 7**, calculate ΔN=8,388,608, or $2^{24}/2$. **Table 1** shows the phase-accumulator values during each clock period and the frequency-generator output—the MSB, D_{23}. This example is a simple divide-by-two stage, but look at the next example.

The second example requires an output frequency of 9,999,998.808 Hz. From **Equation 7**, calculate ΔN=8,388,607, or exactly one count fewer than the previous example's output frequency. **Table 2** shows that over 2^{24} clock pulses, the phase accumulator's MSB, D_{23}, skips one zero-to-one transition and one one-to-zero transition. Thus, the output frequency is 1.192 Hz less than 10 MHz. **Table 2** shows the skips in red.

RESOLUTION AND DYNAMIC RANGE

Now, estimate the output-frequency resolution—how closely you can approach the required frequency. From **Equation 6**, two numbers, ΔN_1 and ΔN_2, define two frequencies, f_1 and f_2:

$$\Delta N_1 = \frac{f_1 2^k}{f_{CLK}};\ \Delta N_2 = \frac{f_2 2^k}{f_{CLK}}. \quad (9)$$

TABLE 1 PHASE-ACCUMULATOR VALUES DURING EACH CLOCK PERIOD

Step	Phase accumulator	D_{23}
0	0	0
1	8,388,608	1
2	0	0
3	8,388,608	1
4	0	0
....	....	......

The minimum step between ΔN_1 and ΔN_2 is one count. Thus, combining two **equations** in **Equation 9**, for the difference between f_1 and f_2:

$$1 = \frac{f_2 2^k}{f_{CLK}} - \frac{f_1 2^k}{f_{CLK}} = (f_2 - f_1)\frac{2^k}{f_{CLK}}, \quad (10)$$

or

$$f_2 - f_1 = \frac{f_{CLK}}{2^k}. \quad (11)$$

From **equations 10** and **11**, you can conclude that frequency resolution does not depend on the target frequency, but on the input-clock frequency and the phase accumulator's binary length.

Now, look at the dynamic range of the frequencies you can obtain. The range of ΔN numbers defines the dynamic range of the generated frequencies, which range from 1 to 2^{k-1}. Applying the above calculations to the earlier example, you can show that the range of frequencies extends from 0.596 Hz to 10 MHz with a resolution of 0.596 Hz.

TABLE 2 MSB SKIPPED TRANSITIONS

Step	Phase accumulator	D_{23}
0	0	0
1	8,388,607	0
2	16,777,214	1
3	8,388,605	0
4	16,777,212	1
5	8,388,603	0
6	16,777,210	1
7	8,388,601	0
8	16,777,208	1
9	8,388,599	0
....	....	......
8,388,605	3	0
8,388,606	8,388,610	1
8,388,607	1	0
8,388,608	8,388,608	1
8,388,609	16,777,215	1
8,388,610	8,388,606	0
8,388,611	16,777,213	1
....	....	......
16,777,214	2	0
16,777,215	8,388,609	1
16,777,216	0	0
16,777,217	8,388,607	0
16,777,218	16,777,214	1
16,777,219	8,388,605	0

Note: Skipped transitions appear in red.

JITTER

Suppose that you want to construct an arbitrary-waveform frequency generator—for instance, an ECG (electrocardiogram)-waveform simulator (**Figure 2**). The memory stores a set of samples that represent one full period of the arbitrary waveform. A circular counter updates the memory address with every sample-clock pulse that comes from the arbitrary-frequency generator. Thus, with every sample clock, the DAC receives a new data sample and updates its output voltage.

Sample-clock jitter is the difference between the time that the sample pulse should appear and the time that it actually appears. Excessive sample-clock jitter would cause waveform distortions in the DAC output. What kind of jitter do you get by using a phase-accumulator-based sample-clock generator? Previous examples show two output frequencies generated from a 20-MHz clock. For simplicity, imagine that the 20-MHz-input-crystal clock has no jitter.

The first example generates a 10-MHz output frequency. You can expect every output-clock

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pulse to arrive exactly 100 nsec after the previous one. From **Table 1**, with every 20-MHz clock pulse, the value in the 24-bit phase accumulator increases by 8,388,608, and, with every input clock, bit D_{23} of the phase accumulator transitions from either one to zero or zero to one, generating a precise 10-MHz frequency with no jitter.

The other example produced a 9,999,998.808-Hz frequency for which the phase-accumulator contents increased by 8,388,607. Starting from Step 2 in **Table 2**, with every clock, bit D_{23} transitions from either one to zero or zero to one, exactly as in the previous example. If so, the transitions occur every 50 nsec and not every 50.00000596 nsec, as required. The transitions are thus a little ahead of schedule. The difference between the two timing intervals—the real and the required—is jitter of 0.596×10^{-14} sec. With the next two clocks, this number doubles, then triples, and so on. As **Table 2** shows, in 8,388,608 steps, the accumulated jitter is equal to an entire input-clock period, or 50 nsec. The clock skips one input-clock transition, as the **table** shows in red, delaying the pulse train by 50 nsec. From this analysis, you can conclude that the input-clock frequency defines the phase-accumulator jitter, which, in essence, is a sampling-frequency error. The higher the clock frequency,

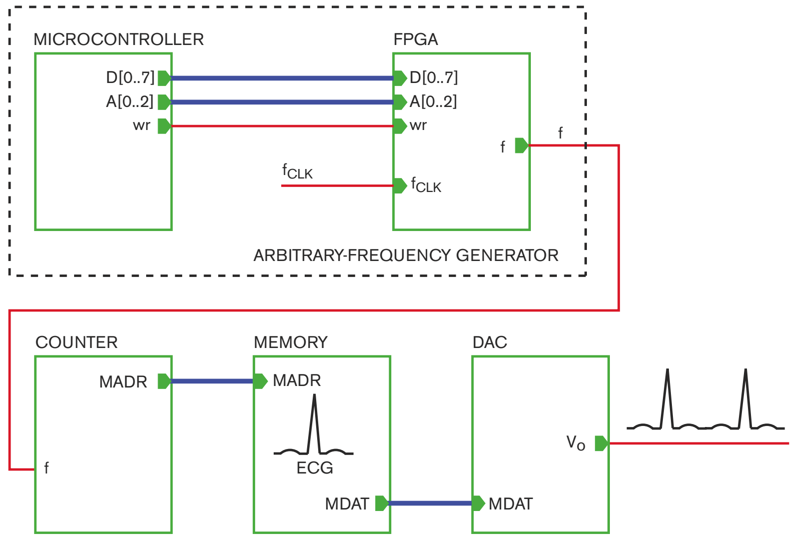

Figure 2 In this arbitrary-waveform frequency generator for an ECG (electrocardiogram)-waveform simulator, the memory stores a set of samples that represents one full period of the arbitrary waveform. A circular counter updates the memory address with every sample-clock pulse that comes from the arbitrary-frequency generator.

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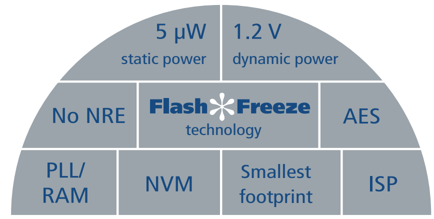

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LISTING 1

```
module fgen ( D, A, wr, fclk, f );

  input  [7:0] D;                        // microcontroller data bus, eight bits
  input  [1:0] A;                        // microcontroller address bus, two bits
  input  wr;                             // microcontroller write signal, active 0->1
                                         // transition
  input  fclk;
  output f;

// -----------------------------------------------------------------------------------
// Interface with microcontroller

reg [15:0] temp;                         // temporary storage register
reg [22:0] dn;                           // ΔN value

 always @(posedge wr)                    // clock data on positive edge of wr signal
  casex (A)
     0: begin                            // store 8 least significant bits
        temp[7:0] = D[7:0];              // into a temporary buffer
      end

     1: begin                            // store 8 middle bits
        temp[15:8] = D[7:0];             // into a temporary buffer
      end

     2: begin                            // store 7 most significant bits and value
        dn[15:0] = temp[15:0];           // of the temporary buffer
        dn[22:16] = D[6:0];              // into ΔN value
      end
  endcase

// -----------------------------------------------------------------------------------
// Phase accumulator based frequency generator

reg [23:0] phase_acc;                    // phase accumulator register

 always @(posedge fclk)
      phase_acc = phase_acc + dn;        // ΔN increase phase accumulator by

 assign f = phase_acc[23];               // assign the most significant bit of
                                         // phase accumulator as an output

endmodule
```

the less jitter you can expect.

Now, add frequency modulation to the arbitrary-waveform generator. It might be a good upgrade to the ECG-waveform simulator, because the frequency modulation can simulate some cases of arrhythmia—a condition in which the heart rate gradually or rapidly changes. To produce frequency modulation, the microcontroller changes the output frequency by periodically clocking out a new ΔN value into the FPGA. As the FPGA receives the new ΔN value, it starts adding this new value to the phase accumulator with each clock, thus causing the output-frequency change to occur immediately.

A phase-accumulator-based arbitrary-frequency generator is easy to implement in an FPGA. The frequency is easy to control—statically and dynamically. The output has highly predictable frequency resolution and low and predictable jitter, suiting it to many applications. EDN

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AUTHOR'S BIOGRAPHY

Eugene Palatnik is president of ITEC Engineering (Pewaukee, WI), a designer and marketer of biomedical-engineering devices—mainly for use in patient monitoring. He holds a master's degree in electrical engineering from Lvov Polytechnic Institute (Lvov, Ukraine), and founded ITEC in 1997. His personal interests include playing the piano and rollerblading with his older son.

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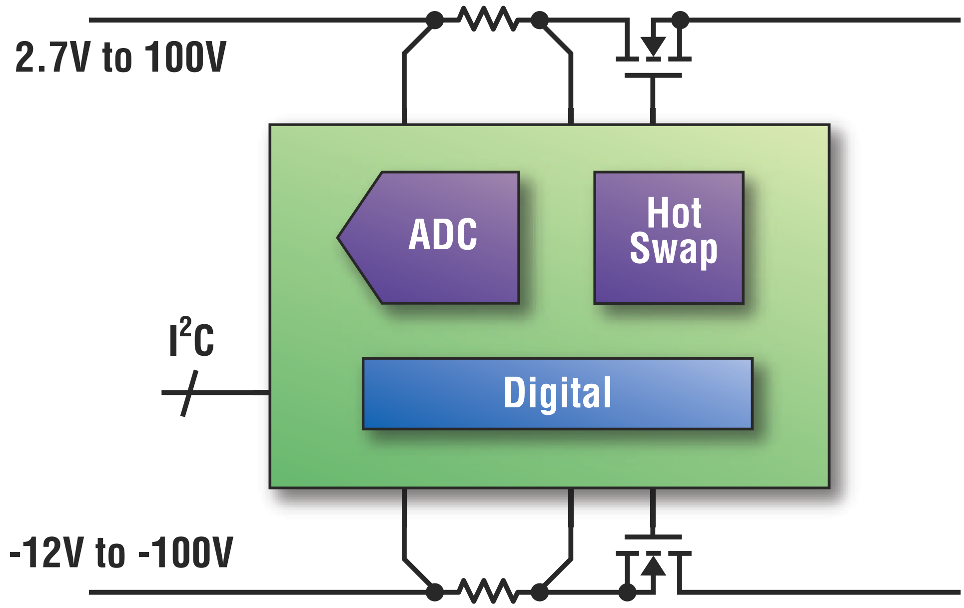

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Nonvolatile digital potentiometer gates logic signal

Reinhardt Wagner, Maxim Integrated Products, Ottobrunn, Germany

This Design Idea describes a simple alternative to a nonvolatile gating function you typically implement using PAL (programmable-array logic), GAL (gate-array logic), or a CPLD (complex-programmable-logic device). To gate a logic signal to block or transmit it, you usually employ a logic gate, such as an AND gate, and use the gate's second input to define whether the gate blocks or transmits the applied signal. Because logic gates perform immediate Boolean operations, their operations are combinational and without memory.

However, if you must program a gate that should always either block or transmit the signal after system start-up, you must store the "transmit/block" logic state in some form of nonvolatile memory. Two basic methods are available for storing such logic states. The first involves using a microcontroller in combination with nonvolatile memory, such as EEPROM. This method is suitable if the system can wait until the microcontroller reads the logic state from memory and applies it to a hardware pin—typically, through a general-purpose I/O pin. Some systems, however, require that the transmit/block signal be present at start-up. For those systems, the read delay from memory is unacceptable.

A second method, which is useful for systems without a microcontroller or that cannot wait for the microcontroller to read from memory at boot time, stores the logic state in a device that makes it immediately available at power-up. For this purpose, PAL devices, GAL devices, and CPLDs implement the gating function in combination with programmable nonvolatile memory. These devices offer more than gating with memory, however, and may be overspecified for systems that need only a few such gates. Also, their packages are relatively large to accommodate the many logic-I/O pins they offer.

If you need only a few nonvolatile gates, consider using a component common in analog- and mixed-signal systems: the digital potentiometer (**Figure 1**). Ground the L end of the resistor string and route the signal into the H end of the string. Then, the wiper output either shorts to ground for blocking or connects to the input signal for transmission.

You can program the digital potentiometer through its serial interface during board or system test. The up/down interface on some digital potentiometers is suitable for that purpose. When selecting a nonvolatile digital potentiometer, you should consider the following criteria:

- Digital potentiometers typically have 32 or more taps; you need at least two. A digital-poten-

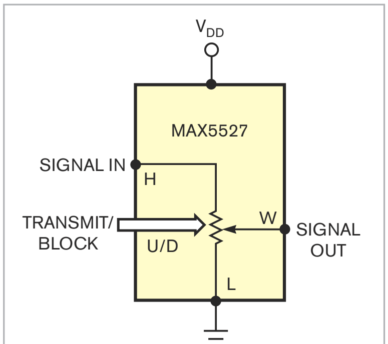

Figure 1 A programmable, nonvolatile digital potentiometer functions as a simple AND gate. Setting the wiper to the device's highest value allows the input signal to propagate to the output; setting the wiper to the lowest value blocks the input signal.

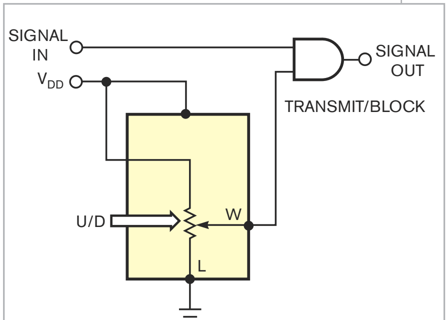

Figure 2 If the bandwidth of the digital potentiometer is too low, you can use the device to drive an AND gate.

tiometer wiper has a resistance associated with the internal switches and should be as small as possible to avoid distorting the switching signal. A typical wiper resistance is 100Ω to 1 kΩ. For the MAX5527 from Maxim (www.maxim-ic.com), wiper resistance measures 90Ω.

- Because the resistance of a digital-potentiometer wiper decreases with increasing supply voltage, you should select a high supply voltage.
- To minimize loading on the signal source and not limit the potentiometer's signal bandwidth, you should select a device with a high end-to-end resistance; 100 kΩ is acceptable for many applications.
- Select a nonvolatile digital potentiometer if you must program the gate's state in nonvolatile memory. Some digital potentiometers are OTP (one-time-programmable); this feature allows you to save the wiper's setting. Using the OTP feature is suitable when you don't expect to make changes in the gating function. The number of gates for which the state must be stored determines the number of potentiometers you need. They are available in arrays of one to six or more per package.

The digital potentiometer's bandwidth determines the maximum data rate for signals transmitted through the potentiometer. If the switching rate of these applied logic signals is too high for the available potentiometers, you can use a conventional, high-speed logic gate with a digital potentiometer controlling the transmit/block input (**Figure 2**).EDN

Soft-limiter circuit forms basis of simple AM modulator

Herminio Martínez, Encarna García, and Juan Gámiz,
Technical University of Catalonia, Barcelona, Spain

One of the most popular circuits for amplitude control in oscillators is the soft-limiter circuit (**Figure 1a**). When the output voltage, $V_{OUT}(t)$, is small, diodes D_1 and D_2 are off. Thus, all of the input current, $V_{IN}(t)/R_1$, flows through the feedback resistor, R_2, and the output voltage is:

$$V_{OUT}(t) = -\frac{R_2}{R_1} V_{IN}(t).$$

This portion is the linear part of the limiter-transfer characteristic in **Figure 1b** with slope of $-(R_2/R_1)$.

On the other hand, when $V_{OUT}(t)$ goes positive, V_A becomes more positive, thus keeping D_1 off; however, V_B becomes less negative. Then, if you continue to decrease $V_{IN}(t)$, you will reach a positive value of the output voltage, at which V_B becomes approximately 0.7V, and diode D_2 conducts. Thus, the positive-limiting value at the output, V_{L+}, is:

$$V_{L+} = \frac{R_6}{R_5} V_{REF} + \left(1 + \frac{R_6}{R_5}\right) V_\gamma,$$

where V_γ is the forward voltage of the diodes—approximately 0.7V. If $V_{IN}(t)$ decreases beyond this value, $V_{OUT}(t)$ will increase, more current is injected into diode D_2, and V_B remains at approximately $-V_\gamma$. Thus, the current through R_5 remains constant, and the additional diode current flows through R_6. Therefore, R_6 appears, in effect, in parallel with feedback resistor R_2, and the incremental gain, A_V, ignoring the diode's resistance, in the positive-limiting region is:

$$A_V = -\frac{R_2 \| R_6}{R_1}.$$

Note that, to make the slope of the transfer characteristic small in the limiting region, you should select a low value for R_6. You can derive the transfer characteristic for positive $V_{IN}(t)$ or negative $V_{OUT}(t)$ in a manner identical to that of the above description. You can easily see that, for a positive $V_{IN}(t)$, diode D_1 plays an identical role to the one that diode D_2 plays for negative $V_{IN}(t)$. So, the negative-limiting level, V_{L-}, is:

$$V_{L-} = -\left[\frac{R_4}{R_3} V_{REF} + \left(1 + \frac{R_4}{R_3}\right) V_\gamma\right],$$

and the slope of the transfer characteristic in the negative-limiting region is:

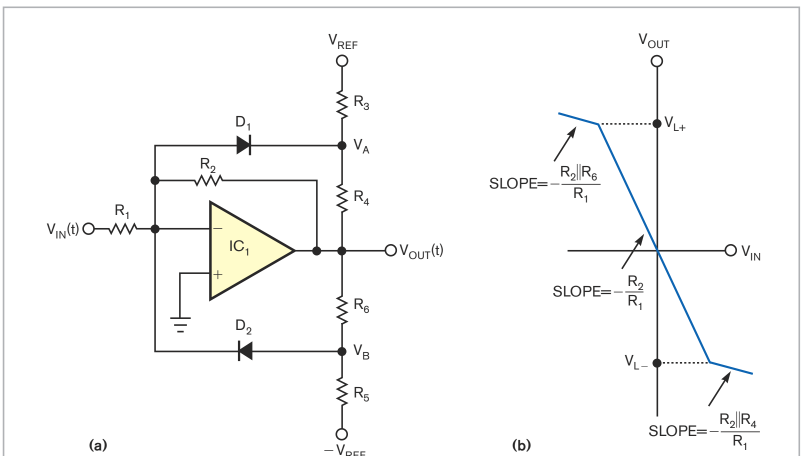

Figure 1 Diodes in the feedback circuit form the basis of this soft limiter (a). The transfer characteristic of the limiter circuit shows inflection points when the diodes begin to conduct (b).

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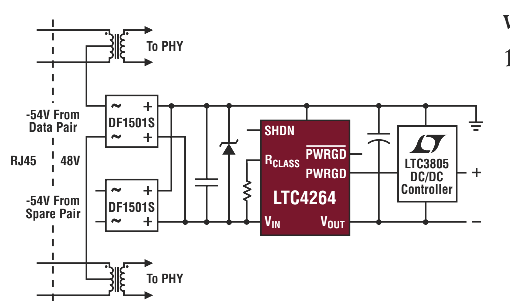

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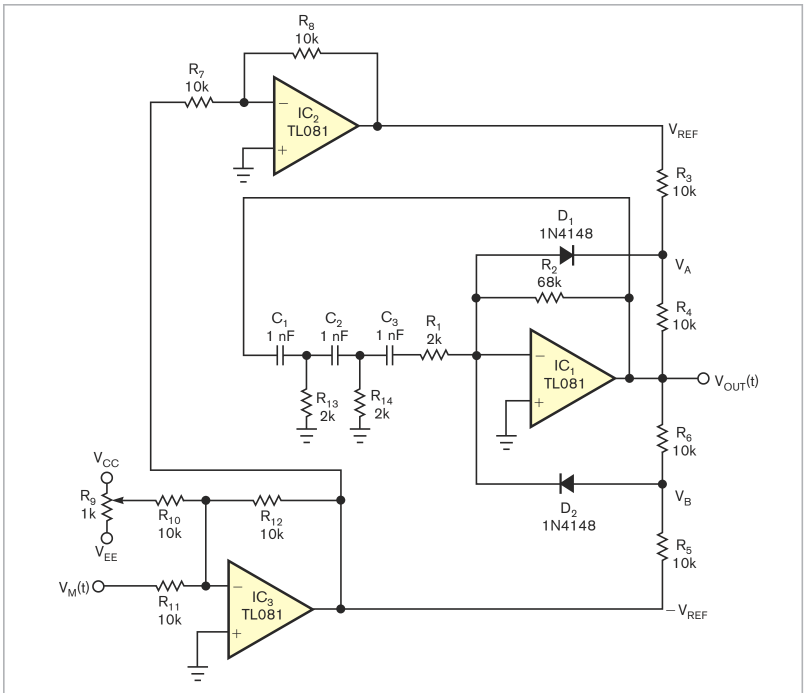

Figure 2 Inserting the soft limiter into the feedback loop of a phase-shift oscillator enables a simple AM modulator.

$$A_V = -\frac{R_2 \| R_4}{R_1}.$$

Note that increasing R_2 results in a higher gain in the linear region and keeps V_{L+} and V_{L-} unchanged. When you remove R_2, the soft limiter turns into a comparator.

Thus, the circuit of **Figure 1a** functions as a soft limiter, and you can independently adjust the limiting levels V_{L+} and V_{L-} by selecting the appropriate resistor values and reference voltages, $\pm V_{REF}$. Therefore, you can use a control voltage to change these limiting levels. You can base a simple AM modulator on this configuration. The RC (resistance/capacitance) phase-shift oscillator in **Figure 2** includes a soft limiter in its voltage amplifier. You can alternatively use any similar RC or LC (inductance/capacitance) oscillator. You can modify the reference voltages, V_{REF} and $-V_{REF}$, with the input modulating voltage, $V_M(t)$. This voltage dynamically adjusts the saturation levels of the oscillator's output. The ratio of the limiter resistors determines the output amplitude and the modulation index.

Figure 3 shows the waveforms of the modulating input, $V_M(t)$, and the oscillator's modulated output, $V_{OUT}(t)$, with the component values of **Figure 2**. In this case, $V_M(t)$ is a sinusoidal waveform with an amplitude equal to 3V, and trimmer R_9 adds a 5V offset voltage. The circuit works in a similar way to a four-quadrant analog multiplier. **EDN**

REFERENCE

1 Sedra, Adel S, and Kenneth C Smith, *Microelectronic Circuits: Fourth Edition*, ISBN 0-19-511663-1, 1998, Oxford University Press, New York.

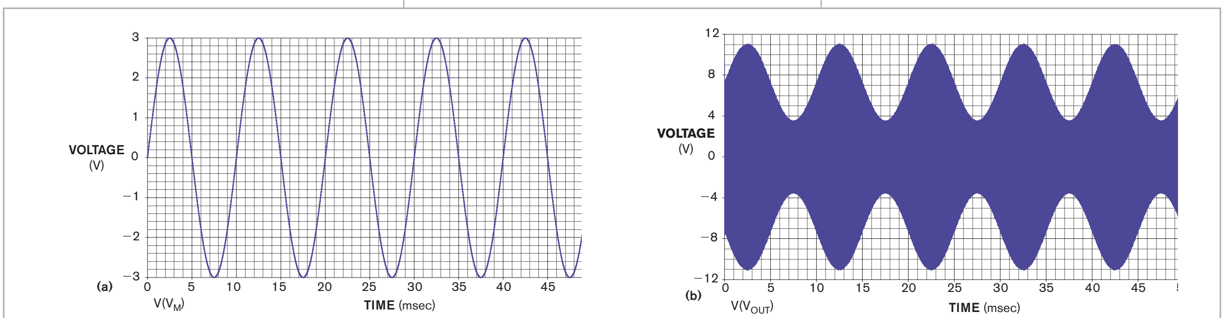

Figure 3 The modulating input, $V_M(t)$ to the circuit in Figure 2 (a) obtains the modulated output voltage, $V_{OUT}(t)$ (b).

Circuits monitor and balance large lithium-ion batteries

Daniel Gomez-Ibanez, Woods Hole Oceanographic Institution, Woods Hole, MA

When using rechargeable lithium-ion cells in large batteries, such as those in an electric vehicle, you encounter unique problems. Bus voltages greater than 100V preclude the use of a standard IC for overcharge and overdischarge protection. In addition, because many cells connect in series, small differences in cells' self-discharge rates eventually lead to unequal levels of charge. Therefore, you must correct the cell balance. This Design Idea provides one strategy for protecting and balancing large, high-voltage batteries. The circuit in **Figure 1** monitors

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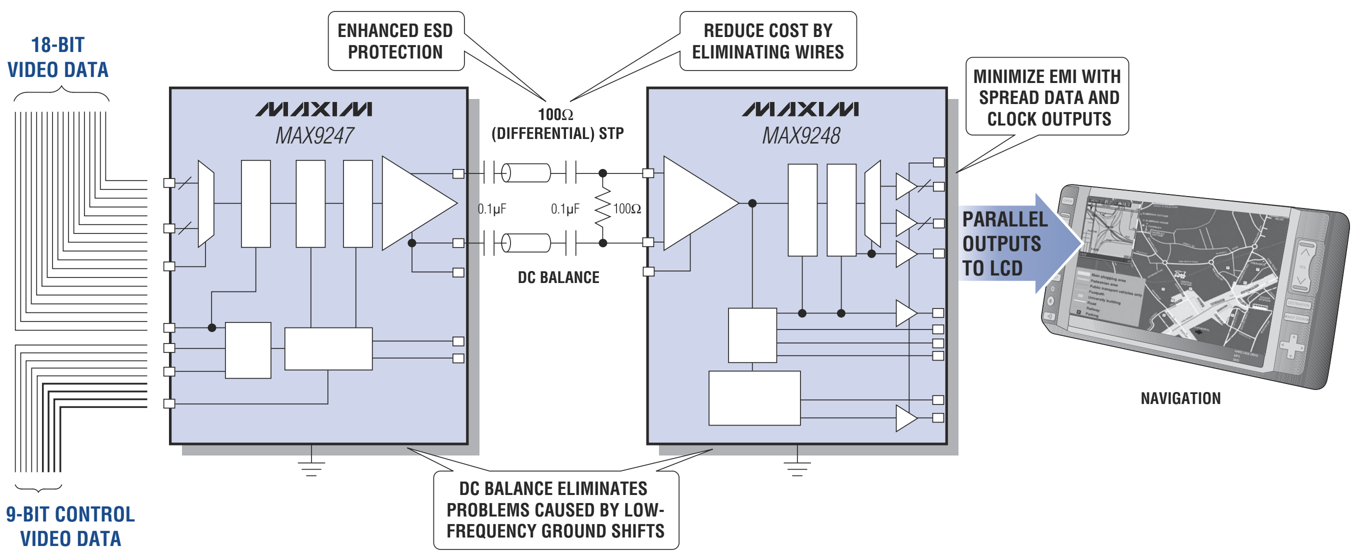
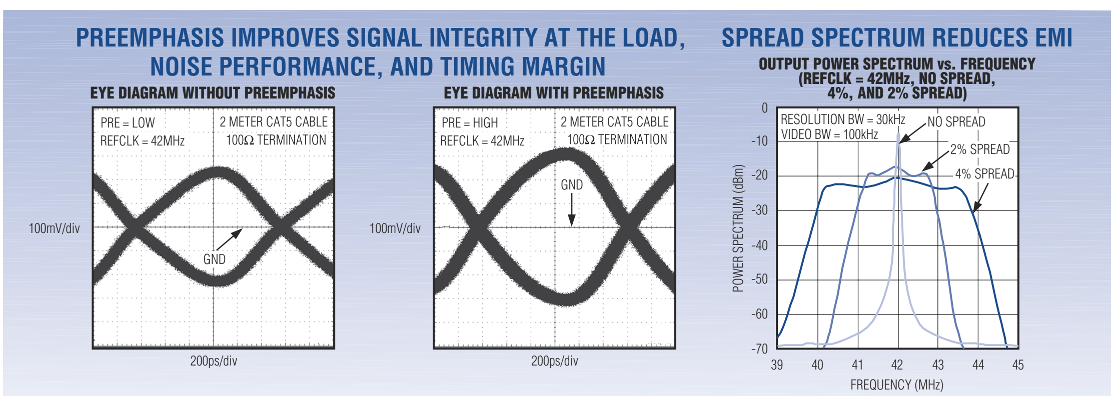




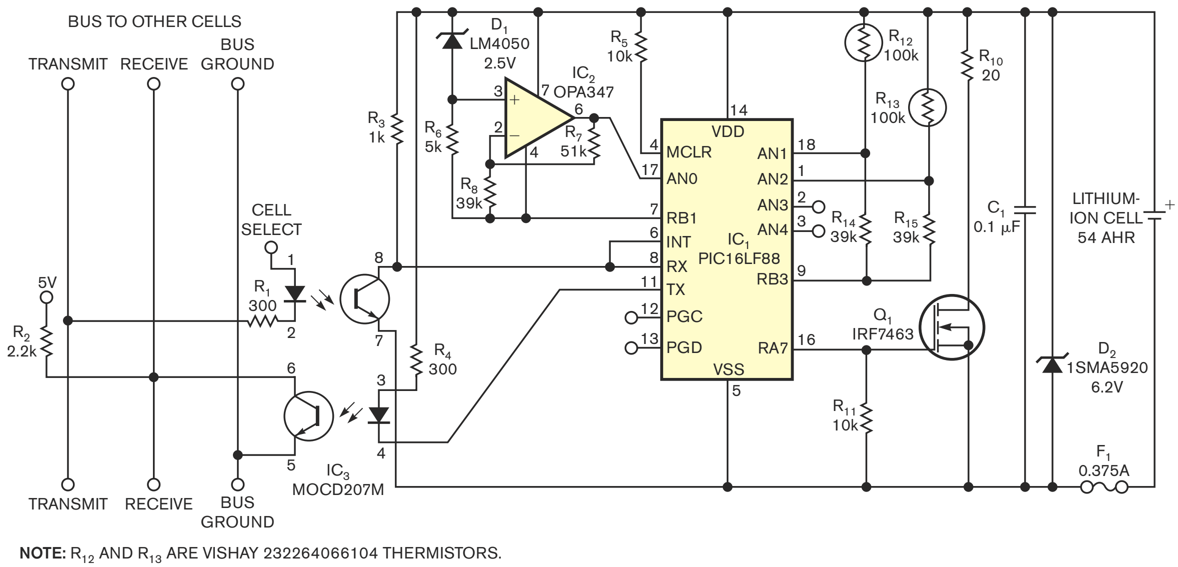


Figure 1 A microcontroller connects directly to a lithium-ion cell and a battery string to monitor the cell's voltage and temperature. This process shunts current through R_{10} under program control to equalize the cell's self-discharge. Each cell in the battery gets its own monitor. The monitors communicate with a controller through optoisolators.

the voltage of a single lithium-ion cell that connects in series in a battery. The circuit communicates with a supervisor processor. The supervisor monitors all cells in the battery, opens a protection switch in case of a problem, and determines where and when balancing is necessary. This approach easily scales to an arbitrarily high bus voltage.

A PIC16LF88 microcontroller gets power directly from the cell voltage, which ranges from 3 to 4.2V. With no need for voltage regulation, the quiescent current of the entire circuit is less than 1 µA, minimizing self-discharge of the battery. Fuse F_1 and zener D_2 protect the monitor from high voltage in the unlikely event that the cell becomes disconnected from the battery. An optocoupler connects between the cell monitor and an asynchronous serial bus, running at 9600 baud. A cell-select line, driven by the supervisor, selects one cell at a time. The MOCD207M optocoupler has a tightly toleranced current-transfer ratio, so it operates predictably over the possible range of supply voltages. Although the quiescent current of this isolator is near zero, the supervisor can wake up the monitor from sleep at any time by sending a pulse over the serial line.

The monitor measures cell voltage by measuring the fixed voltage of the LM4050 with respect to the unknown supply. Op amp IC_2 scales the signal to achieve 3-mV resolution using the microcontroller's built-in 10-bit ADC. The reference, op amp, and gain error introduce voltage offsets, which you can calibrate in software. The remaining error arises from temperature variation of these parameters. R_7 and R_8 use a temperature coefficient of 25 ppm/°C. The resulting accuracy of the voltmeter is ±7.5 mV over 0 to 50°C. By biasing the reference from a digital output, the voltmeter draws current only when necessary. The same trick biases several thermistors, which measure the temperature of the monitored cell.

This cell monitor can balance an overcharged cell by shunting 200 mA through R_2. Although the shunt current is smaller than the battery's maximum discharge current of 12A, it is more than enough current to balance the differential self-discharge of series-connected cells.EDN

White-LED driver operates down to 1.2V supply voltage

Dave Wuchinich, Modal Mechanics, Yonkers, NY

Many LED drivers, using both charge pumps and inductors, are available to boost the 1.2 to 2.4V available from single- and dual-cell NiMH (nickel-metal-hydride) batteries to the 3.6V that white LEDs require. However, most of these circuits, such as the Maxim (www.maxim-ic.com) MAX1595, require a minimum input voltage of approximately 2.5V to operate properly. The MAX1595 works with an input voltage of 2.4V but does not ensure an adequate output until the input voltage reaches approximately 3V. Furthermore, as the battery voltage decreases to the threshold level, the output becomes erratic. The circuit in **Figure 1** uses a flip-flop

to generate flux in an inductor, which then charges a capacitor in the common boost configuration. US Patent 4,068,149 describes the flip-flop's operation in an application for operating an incandescent safety lamp's flasher (**Reference 1**).

In **Figure 1**, R_1 provides a path for starting current through the base-emitter junctions of Q_1 and Q_2. Q_2 thus turns on and, in so doing, turns on Q_1, rapidly forcing both transistors into saturation. However, C_1 charges through R_2 to the battery voltage minus the base-emitter drop of Q_1 and the saturated collector-emitter voltage of Q_2, eventually causing Q_1 to turn off and thereby also turning off Q_2. C_1 then discharges through R_1 and R_2 and the forward-biased base-collector junction of Q_2. The R_2C_1 time constant determines the turn-on time, and $(R_1+R_2)(C_2)$ determines the turn-off time. C_2 acts as the capacitive input filter for the current flowing from L_1 when Q_2 is off and provides a substantially constant voltage to power D_2, a standard white LED.

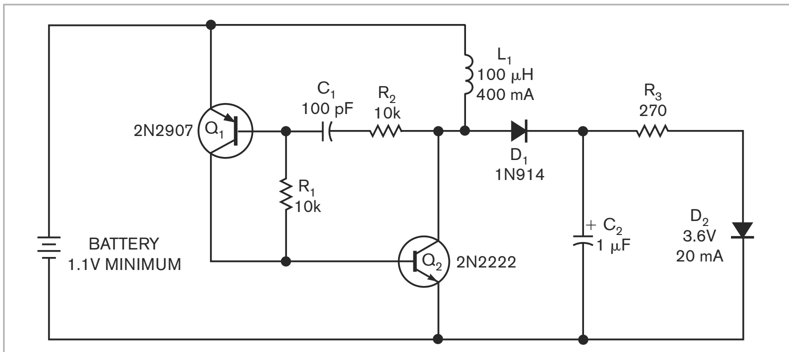


Figure 1 In this circuit, transistors Q_1 and Q_2 form a flip-flop that toggles at 60 kHz, providing a drive current for the output LED down to the 1V battery voltage.

The output voltage is proportional to the battery voltage.

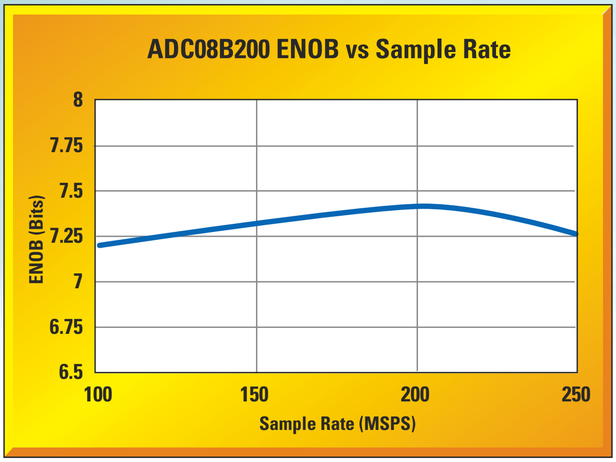
With the component values in **Figure 1** and with L_1, a Coilcraft (www.coilcraft.com) MSS7341-104MLB, the operating frequency is approximately 60 kHz. With a battery voltage of 2.36V from two NiMH cells, approximately 20 mA of current flows through the LED. In tests simultaneously driving two LEDs, each with its own current-limiting resistor, R_3, the energy-conversion efficiency of the circuit at this battery voltage is approximately 80%. Operation continues with battery voltages of slightly more than 1V, and the delivered current diminishes but still provides usable illumination.EDN

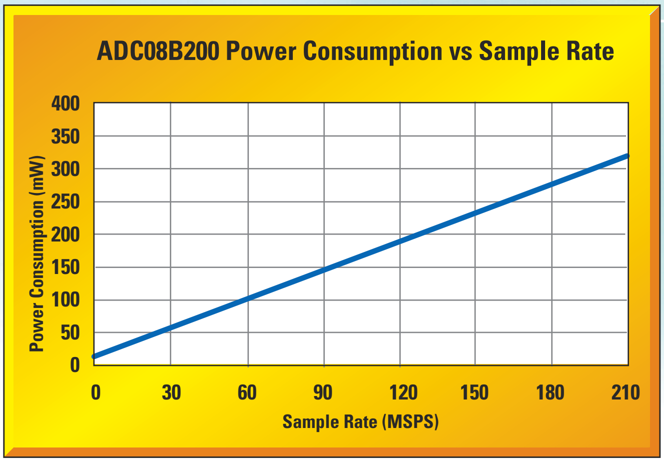
REFERENCE

1 Wuchinich, David G, "Flasher circuit with low power drain," US Patent 4,068,149, Oct 28, 1975, http://patft.uspto.gov.

8-Bit, 200-MSPS ADC with 1K Capture Buffer

ADC08B200 On-Chip Buffer Enables FPGA Design Flexibility





ADC08B200 Features

- Selectable buffer size for flexibility
- On-chip PLL provides option to multiply input clock signal frequency by 2, 4, or 8 times, allowing for slower on-board clock
- Direct access to internal reference ladder allows for flexibility in input voltage ranges
- Power consumption scales linearly with sampling rate
- FPGA training pattern simplifies high-speed data capture

Product ID	Sampling Rate	Power	ENOB (Bits)	SNR (dB)	SFDR (dB)	THD (dBc)	Packaging
ADC08B200	200 MSPS	2 mW/MSPS	7.4	47	56	-55	TQFP-48
ADC08200	200 MSPS	1.05 mW/MSPS	7.4	46	58	-58	TSSOP-24
ADC08100	100 MSPS	1.3 mW/MSPS	7.5	47	60	-60	TSSOP-24

Ideal for use in laser ranging, RADAR, pulse capturing, flat panel displays, projection systems, set-top boxes, battery-powered instruments, communications, medical scan converters, X-ray imaging, high-speed Viterbi decoders, and astronomy applications

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DESIGN NOTES

Ultraprecise Current Sense Amplifier Dramatically Enhances Efficiency and Dynamic Range – Design Note 423

Jon Munson

Introduction

Accurate current measurement is indispensable in many electronic systems. The current is usually measured by amplifying the voltage it generates across a small value resistance. For systems that require a large dynamic measurement range, the sense resistance must be increased or the precision of the amplifier must be improved. Increasing the value of the sense resistor has the detrimental effect of increasing power dissipation. The better option is to improve the precision of the sense amplifier.

Amplifier precision depends a great deal on the input offset voltage of the amplifier. Historically, current sense amplifiers on the market offered input offset voltage performance on the order of hundreds or even thousands of µV. With such parts, achieving a practical dynamic range of 8 to 10 bits can cost more than a Watt of power dissipation at full operating current. The LTC®6102 ultraprecise current sense amplifier reduces input error to a miniscule 10µV. This dramatic performance enhancement translates directly into a greater measurement dynamic range—16 bits is possible even while *lowering* power dissipation in the sense resistor—thus greatly expanding the gamut of current sensing design options.

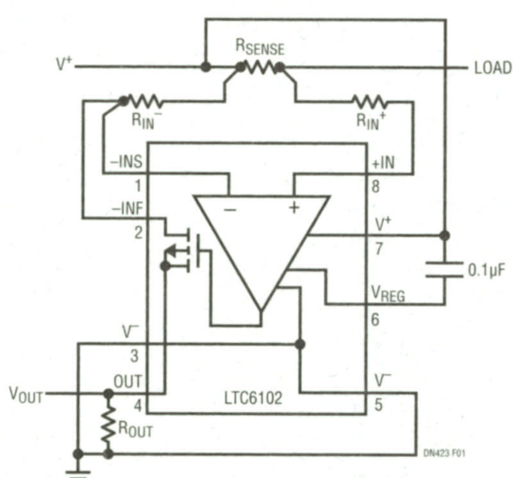

Figure 1. Ultraprecise Current Sensing with LTC6102

Precision Buys Efficiency

The LTC6102 is easily connected as shown in Figure 1.

The input voltage is developed by the sense resistor, and the voltage gain of the amplifier is set by the input and output resistors. The overall scaling is simply:

$$V_{OUT} = I_{LOAD}\left(R_{SENSE} \bullet \frac{R_{OUT}}{R_{IN^-}}\right)$$

The accuracy at small load currents is primarily set by the input offset voltage V_{OS}. The current measurement error I_{OFFSET}, due to the V_{OS}, is given by:

$$I_{OFFSET} = \frac{V_{OS}}{R_{SENSE}}$$

For a given current offset accuracy requirement, it can be seen that with a low V_{OS} that R_{SENSE} may be reduced accordingly, to sub-milliohms in many applications.

In most applications the circuit gain is selected so that V_{OS} translates to about 1LSB (least significant bit) in the analog-to-digital (ADC) acquisition system. Dynamic range is dictated by the maximum signal amplitude that the ADC can handle and how much power the R_{SENSE} resistor is permitted to dissipate.

Consider a comparison between two 8-bit sense amplifier solutions, one using a typical amplifier with V_{OS} = 500µV and one using the LTC6102, where V_{OS} = 10µV. The resolution of each is 20mA. The higher offset part requires a sense resistor of at least 25mΩ, whereas the LTC6102 only requires 500µΩ. At 5A, nearly full-scale current for this example, the R_{SENSE} power loss is 625mW with the higher offset part, but just 13mW with the LTC6102, a 98% reduction in wasted power.

Print Your Own Sense Resistors

With the ultralow sense resistance capability offered by the LTC6102, the printed circuit foil itself can be used as a practical sensing element. A circuit board using 1oz

copper has a nominal sheet resistivity of 500 /square. The value drops proportionally for thicker foils and rises for thinner foils. A trace of width W and length L (in any identical units) has the following resistance:

$$R_{SENSE} \approx 500\mu\Omega \bullet \frac{L}{W}$$

The length of the resistor is simply the spacing between the Kelvin taps along the trace. One ounce copper can generally carry up to about 100mA/mil of trace width (or 4A/mm), which constrains the minimum size of the resistor structure. Another constraint is reproducibility, so the larger, the better. Ultimately the thickness tolerance and tempco of the copper limit the accuracy a printed resistor can have.

Figure 2 shows a printed structure for the 5A circuit example discussed previously. In this layout, the L/W factor is set to 1 (for R_{SENSE} = 500μΩ) and the size is dictated mainly by the accuracy of printed circuit etching.

Using copper for the sense resistance means that the scaling of the circuit is nearly proportional to absolute temperature, about +0.4%/°C at room temperature. In applications where the current is being monitored for overload protection, the tempco may be convenient, in that a fixed protection threshold will automatically correspond to lower current at higher temperature. For stable measurements, a software calibration and temperature correction approach can be used, or the tempco can be compensated by using a copper-based resistor for R_{IN}^-, such as a small surface mount inductor with known resistance properties (>10Ω readily available, e.g. Vishay IMC series).

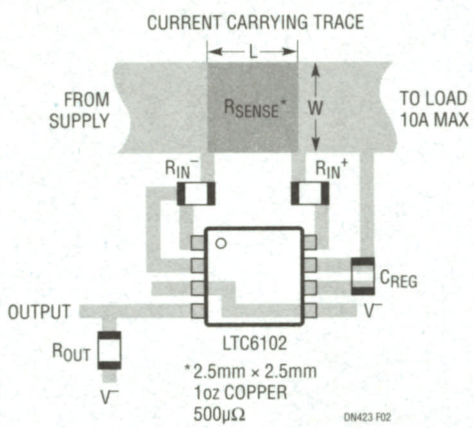

Figure 2. LTC6102 Layout Using Printed Sense Resistance

Design Tips and Details

If you are not printing your own sense resistors, and need the accuracy of off-the-shelf components, be sure to specify 4-wire (Kelvin) sense resistors for best results. Such resistors are designed so that the resistance is well calibrated between the sensed taps, thus eliminating the error from solder resistance in the load path.

Accurately measuring microvolt level signals raises the real possibility of stray thermocouple effects due to dissimilar metallic interconnections. Figure 1 shows the use of an R_{IN}^+ that is generally identical to R_{IN}^-. The purpose of this extra resistor is to provide identical metallurgical conditions to both amplifier inputs for minimizing thermocouple effects, as well as to minimize DC bias current imbalance.

The R_{IN}^- value is selected to conduct about 500μA at times of peak measured current I_{PEAK}. The voltage drop on R_{IN}^- is equal to the voltage drop on R_{SENSE}, so:

$$R_{IN^-} \geq \frac{I_{PEAK} \bullet R_{SENSE}}{0.0005}$$

Gain accuracy of the overall circuit is established mainly by the quality of the resistors used. This allows the designer to optimize the cost vs performance tradeoff in each specific application.

To minimize copper loss errors in the feedback loop of the LTC6102, the inverting sense input (–INS) and the inverting feedback connection (–INF) have been kept separate so that a Kelvin connection to R_{IN}^- can be made. This connection can also be seen in the suggested layout of Figure 2.

Figure 2 shows the V^+ connections tied to the load side of R_{SENSE}, whereas Figure 1 shows a tie-in to the supply side. The LTC6102 will work in either configuration. The difference is that the Figure 2 connection will also include the LTC6102 quiescent supply current (300μA typically) in the measured load current. Supply voltages from 4V to 100V are supported.

Conclusion

The LTC6102 is the industry's highest precision current sense amplifier. The exceptional accuracy allows for dramatic reduction in the R_{SENSE} resistance, thereby improving efficiency, dynamic range and current handling.

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productroundup

POWER SOURCES

Power supplies target medical applications

The NV-175M configurable ac/dc power supplies have a 4-kV ac input-to-output isolation. Meeting IEC 60601 international safety standards, the devices suit use in patient-connected medical applications. The supplies include PFC (power-factor correction), 90% efficiencies, and 180W-typical and 200W-peak output-power ratings. Four standard models are available, as well as custom configurations including one to three outputs with 3.3, 5, 12, 15, and 24V-dc output voltages adjustable to 28V. Measuring 1.3×3×5-in. without a cover or fan, the NV-175M costs $126 (100).

Lambda, www.lambdapower.com

Reliability tester qualifies components for high-reliability applications

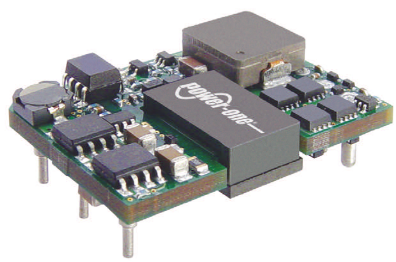
The SEMTest power-semiconductor-test system performs accelerated lifetime testing of power semiconductors and modules using IGBT (insulated-gate-bipolar-transistor), MOSFET, SCR (silicon-controlled-rectifier), diode, and bipolar parts. You can configure the system with 20 to 1000 test cells, and larger systems are available by special order. Each of the stress-screening reliability tester's cells features a local controller to set and monitor applied or UUT (unit-under-test) power and other test parameters. The system provides a measurement unit for temperature, current, voltage, and timing; allows complete characterization and production tests to accelerate failure mechanisms of individual devices; and determines functional operating limits. Features include power cycling for thermal and electrical stressing of devices under test, trend monitoring with user-defined warning and control limits, rapid device-temperature cycling and ambient-temperature

productroundup

POWER SOURCES

profiling, nascent-failure detection, and automatic alert sending. The system also measures junction temperatures. The SEMTest stress-screening reliability tester costs $100,000.

Intepro Systems, www.inteproate.com



16th-brick converter claims efficiency boost of more than 90%

Providing a 3.3V output voltage, the 20A SSQE48T20033 isolated dc/dc 16th-brick converter boosts power densities as high as 56W/in.[2] and increases efficiency to more than 90% in communications, data/server/storage, and workstation applications. Features include onboard input differential-LC filtering, start-up into prebiased loads, a 10%/−20% output trim, a 36 to 75V input-voltage range, and the ability to withstand a 100V input transient for 100 msec. Interface capabilities include remote sense and remote on/off with a positive- or negative-logic option. The device also features overtemperature, output-overvoltage and -overcurrent, and input-undervoltage protection. Available with a 0.374-in. profile, the SSQE48T20033 costs $25 (1000).

Power-One, www.power-one.com

USB/ac-adapter chargers withstand 30V dc or 16V USB input voltages

Suiting one-cell lithium-ion batteries, the high-voltage, dual-input, stand-alone MAX8804Y and MAX8804Z USB/ac-adapter chargers provide protection by shutting off input voltages greater than 7.5V, withstanding an input voltage as high as 30V dc or 16V USB, and integrating thermal-regulations circuitry. The devices feature intelligent USB/dc-input circuitry that can automatically select either a USB- or an ac-adapter input source. The chargers integrate two high-voltage, low-on-resistance charging FETs, a reverse-current-blocking diode, a current-sensing resistor, and input-overvoltage-protection circuitry. The MAX8804Y provides a fast-charging start without a precharging stage, and the MAX8804Z uses a prequalification charging stage bringing battery voltage to 2.5V. Measuring 6×6 mm in a TDFN package, the MAX8804Y and MAX8804Z cost $1.40 (2500) each.

Maxim Integrated Products, www.maxim-ic.com

Switching power supplies provide EMC performance

The ultraminiature, encapsulated ECA Series switching power supplies comply with EN 60601-1-2:2001 requirements for EMC-noise compliance. Accepting 90 to 264V-ac universal inputs, the series also features 60 models providing 5 to 15W output power with 5 to 24V-dc single and dual outputs. The series comes in pin-mounted printed-circuit-board plug-in or screw-terminal-chassis mounting. Measuring 2.28×1.77×0.83-in. for the 5W version, the ECA Series power supplies cost $29.

Astrodyne, www.astrodyne.com

Encapsulated regulator system suits military and avionics applications

The LTM4600HVMPV encapsulated, 10A switching dc/dc-regula-

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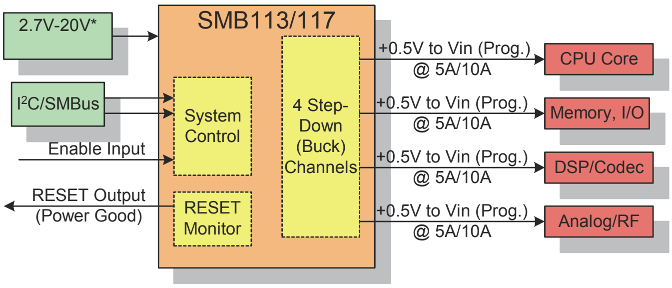
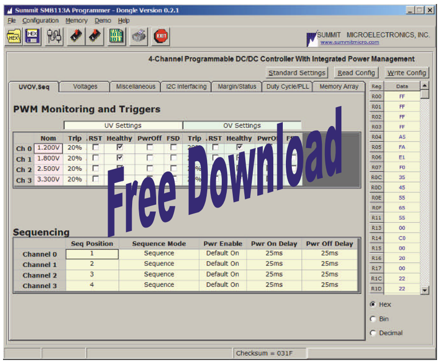
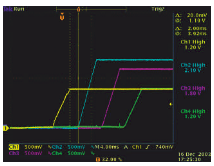




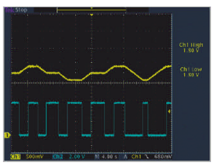
Develop device with convenient programming tool and upload HEX file

-Summit ships pre-programmed "custom" units in high volume

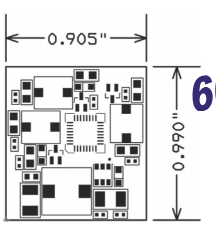


Sequencing

Integrated Power Control



Dynamic Output Voltage



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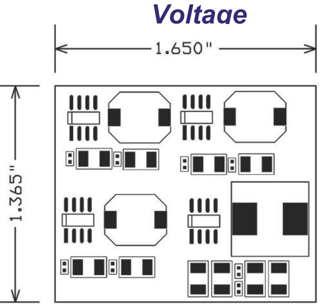

Summit Solution (<1 in²)

Competitor's Solution (2.25 in²)

Features/Parameters	SMB113B	SMB113A	SMB117	SMB117A
Max Output Current (A)	2	5	7.5	10
Switching Frequency (kHz)	1000	800	400	250
Step-Down Outputs	4	4	4	4
Control Interface	I²C	I²C	I²C	I²C
Input Voltage Range (V)*	2.7-6.0	2.7-6.0	2.7-6.0	2.7-6.0
Output Voltage Range (V)	0.5-VIN	0.5-VIN	0.5-VIN	0.5-VIN
Typical Efficiency	>90%	>90%	>90%	>90%
Source/Sink "DDR" Mode	Y	Y	Y	Y
Operating Temp Range (°C)	-40 to +85	-40 to +85	-40 to +85	-40 to +85
Package Size (mm)	5x5	5x5	5x5	5x5
Package Type	QFN-32	QFN-32	QFN-32	QFN-32

Features

- +2.7V to +20V*
- ± 1.5% Output Voltage Accuracy
- >90% Efficiency
- I²C + Programmable Configuration
- Dynamic Output Voltage Control
- Pushbutton Enable Input
- Programmable FET Driver "Deadtime"
- Programmable Enable/Seq/Slew Rate
- UV/OV Monitors with RESET Control
- +0°C to +70°C or –40°C to +85°C

Applications

- Cable/Satellite/DVR Set-Top Boxes
- Digital HDTV
- Slimline Notebook PC's
- SOHO Networking Equipment
- Automotive/Marine Navigation

*For higher input voltages up to +20V – contact factory

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tor system targets military and aerospace systems. Part of the μModule dc/dc regulator family, the regulator system is tested over a −55 to +125°C temperature range. The synchronous-switch-mode dc/dc step-down regulator features a built-in inductor, supporting power components and compensation circuitry. Operating from a 4.5 to 28V input-supply range, the device regulates a 0.6 to 5V output voltage and delivers a 10A continuous load current with a 14A peak, claiming 92% efficiency. The device requires input and output bulk capacitors and a resistor for setting the output voltage. Available in a 15×15×2.8-mm military-grade, plastic LGA housing, the package provides lower thermal impedance than similarly sized BGA packages. The LTM4600HVMPV costs $36.95 (1000).

Linear Technology, www.linear.com

MICROPROCESSORS

Microkernel targets the NEC Electronics V850 microcontroller

The μ-velOsity RTOS (real-time-operating-system) microkernel targets NEC Electronics' V850 embedded-microcontroller family. Features include a 2-kbyte ROM footprint, a 1-kbyte RAM footprint, and 30-cycle service-call times. The microkernel also includes complete kernel source code and Multi's kernel-aware debugging and project-creation wizard. The μ-velOsity costs $9500 and has no royalty charger per unit.

Green Hills Software, www.ghs.com

AVR microcontrollers reduce power consumption in sleep modes

Joining the vendor's 32-pin picoPower AVR microcontroller family, the ATmega48P, ATmega88P, ATmega168P, and ATmega328P devices have 4, 8, 16, and 32 kbytes of flash memory, respectively, providing a 28- to 100-pin range and a 4- to 64-kbyte flash-memory range for the family. The devices consume 340 μA in active mode at 1.8V operating from a 1-MHz internal RC oscillator, 650 nA in power-saving mode with a real-time counter, and 100 nA in power-down mode. The picoPower AVRs are pin-, performance-, and code-compatible with previous-generation AVR microcontrollers. Features include a 32-kHz crystal oscillator, automatic disabling and re-enabling of brownout detection, sleeping BOD (bandwidth-on-demand) circuitry during sleep mode, a PRR (power-reduction register) that completely powers down peripherals, and digital-input registers for removing leakage on ADC input pins. Operating from 1.8 to 5.5V, the microcontrollers feature a 10-bit ADC, a USART, an SPI (serial-peripheral interface), a two-wire interface, an internal temperature sensor, and 20-MIPS throughput at 20 MHz. The ATmega48P, ATmega88P, ATmega168P, and ATmega328P cost $1.18, $1.65, $2, and $2.65 (10,000), respectively.

Atmel, www.atmel.com

32-bit CISC microcontrollers provide 50-MIPS performance

Adding 12 devices to the vendor's 32-bit H8SX CISC (complex-instruction-set-computer)-microcontroller family, the H8SX/1658R, H8SX/1668R, H8SX/1558, and H8SX/1568 devices provide as much as 1 Mbyte of on-chip flash memory, 64 kbytes of SRAM, and 50-MIPS operation. The units provide high-speed-serial, USB, and par-

MICROPROCESSORS

allel-bus interfaces and power-down modes for wake-up by multiple external interrupts. The 1658R and 1668R drive VGA TFT (thin-film-transistor)-LCD panels running at 65 frames/sec, and a TFT-LCD interface directly drives the LCD panel. These devices also support updates to the external frame buffer during LCD-panel operation. Three models in the 1658R group and three in the 1668R group feature 384, 512, or 1024 kbytes of on-chip flash memory operating from a single power supply and allowing access to the processor in a single clock cycle. These groups also support USB 2.0 device functionality using an on-chip peripheral. The 1558 and 1568 groups feature 5V interfaces and two or three high-speed, 10-bit ADCs with 2-μsec conversion times. Using the on-chip timers, the sampling of the ADCs can interleave at a 1.5M-sample/sec rate at 5V operation. Additional features include two channels of SCI (serial-communication interface), an 8-bit timer, an 8-bit DAC, a DMA (direct-memory-access) controller, and an I^2C-bus interface. System engineers can use the USB-bus powered E10A-USB emulator as a development environment. Compatible with the vendor's previous models, the 1658 and 1658R come in LQFP-120 packages, and the 1668 and 1668R come in LQFP-144 packages. Prices for the H8SX/1658 range from $12.15 to $16.20, and prices for the H8SX/1658R range from $12.15 to $15.40.
Renesas Technology America, www.renesas.com

Microcontroller with integrated RTC drives LCDs

Providing a digitally trimmable RTC (real-time clock) with a dedicated backup battery pin and an LCD interface supporting 160 segments, the MAXQ3100 mixed-signal microcontroller suits industrial, medical, and consumer applications requiring an RTC and an LCD controller. The microcontroller also features a FLL (frequency-locked loop), two analog comparators, and a digital temperature sensor. Additional peripherals include a 16-kbyte EEPROM, a 1-kbyte data SRAM, a watchdog timer, two USART serial ports, and three timers. The evaluation kit includes an onboard LCD and a JTAG-interface board for communication with a computer. The IDE includes a debugger, an assembler/linker, a time-limited version of the IAR C compiler, and a simulator. Available in an 80-pin MQFP, the MAXQ3100 microcontroller costs $3.19 (1000).
Maxim Integrated Products, www.maxim-ic.com

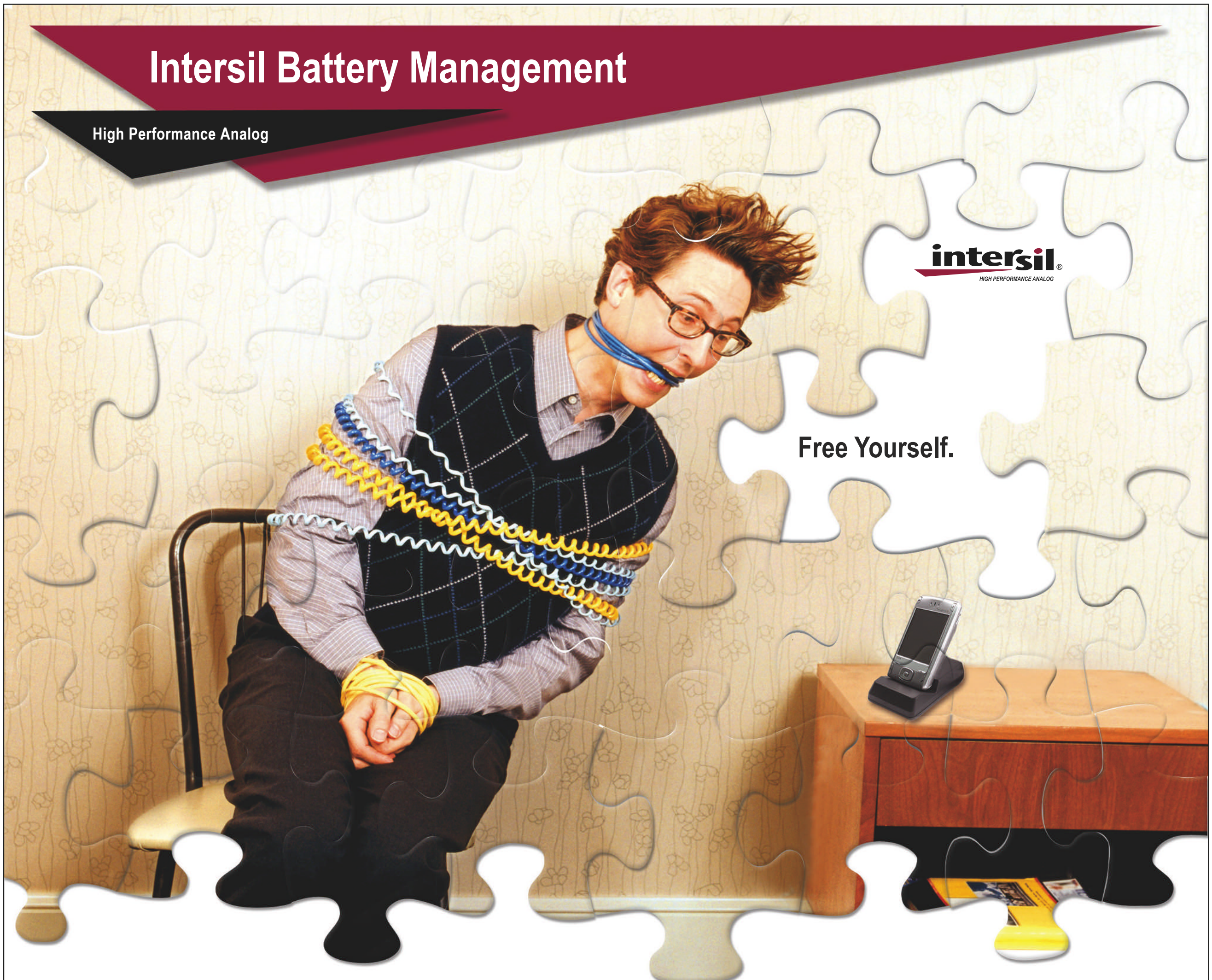
EMBEDDED SYSTEMS

FPGA-based processing board performs SDR functions

The StreamBlade MiniFX FPGA-based processing board receives streaming-data IF samples from two ADCs, provides SDR (software-defined-radio) functions, computes steering vectors for direction finding, and provides results using gigabit Ethernet. Using 128 Mbytes of DDR2 SDRAM allows the use of MiniFX as a dual PPC405 processing board, a pure-FPGA processing board, or a combined hardware/software boundary processor. Using Ethernet for implementing distributed computer backplane, configuration, and control, the board allows use of the configured Xilinx Virtex-4 FPGA available with an FX20, FX40, or FX60. The device features support for a 10/100/1000 Ethernet port, two serial ports, and a variety of LVDS (low-volt-

Intersil Battery Management

High Performance Analog



Intersil's Li-Ion/Li-Polymer Battery Charger provides **28V protection for both cradle AND USB charging.**

ISL9214 Key Features:

- **28V protection for both cradle and USB input** allows users to utilize low-cost, large output tolerance adapters.
- **Charge current Thermaguard™** protects IC against over-temperature events.
- **Programmable charge current/end-of-charge current** allows designer to customize to exact requirements.
- **Fixed 380mA USB charge current** prevents exceeding USB max charge current.

The ISL9214 allows the flexibility to use either fast-charging rates of an AC adapter or the convenience of a USB charger.

Cradle Input: The max input voltage tolerance is 28V, programmable end-of-charge current, and the included end-of-charge latch is the default input source.

USB Input: Takes input from USB port or other low-voltage supply, fixed charge current at typically 380mA, and only charges when cradle source is not connected.

End-of-charge indicator is latched, based on completed charge.

When the battery voltage falls below minimum spec, the charger operates with a trickle charge current of 14% of the programmed cradle input or at 53mA for USB power.

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age-differential-signaling) connectors, enabling direct user-configurable access to the FPGA. Measuring 3.5×3-in., the MiniFX processing boards cost $2500 in the FX60 FPGA configuration.

Embedded Systems Design, www.embedded-sys.com

Embedded-panel computer has a 1-GHz Celeron M processor

Powered by a 1-GHz Intel Celeron M processor, a 915GME+ICH6-M chip set, and 533-MHz DDR2 SDRAM with a capacity as great as 512 Mbytes, the NuPPC-0701T embedded-panel computer features a 7-in.-touchpanel LCD and a fanless low-power design. Data-storage and connectivity options include a CompactFlash slot, three USB ports, and 10/100BaseT gigabit-Ethernet ports. The HMI (human-machine-interface) display supports 800×480-pixel resolution with 400-cd/m^2 brightness. The NuPPC-0701T embedded-panel computer costs $1495.

Adlink Technology, www.adlinktech.com

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LOOKING AHEAD

TO THE ARM DEVELOPERS' CONFERENCE

The annual event for users of the ARM microprocessor architecture kicks off Oct 2 in Santa Clara, CA, and just looking at the subjects of the technical tracks gives some idea of the scope of ARM applications. Sessions range from techniques for SOC (system-on-chip) design to implementing ARM cores in FPGAs, from multimedia-hardware design to multiprocessing systems, and from software-based virtualization to system security. Even if you are not using ARM processors, you couldn't ask for a more concentrated review of modern microcomputing-design technology than you would get by attending a selection of presentations at this three-day symposium.

LOOKING BACK

AT HOME POWER-LINE NETWORKING CIRCA 1957

Signals generated by a small transmitter and carried over household electrical wiring provide controls for channel switching and sound muting of TV receivers. The carrier current provides the necessary power to operate the transmitter and supplies a direct path for the signal. The Westinghouse-developed system uses two carriers. A continuous wave activates both channel-selection and muting relays on the TV receiver. A modulated wave activates only the sound-muting relay. Transmitter output is in the order of 12 mW continuous. The input circuit receives any of four carrier frequencies in the 50- to 75-kilocycle range.—*Electrical Design News*, September 1957

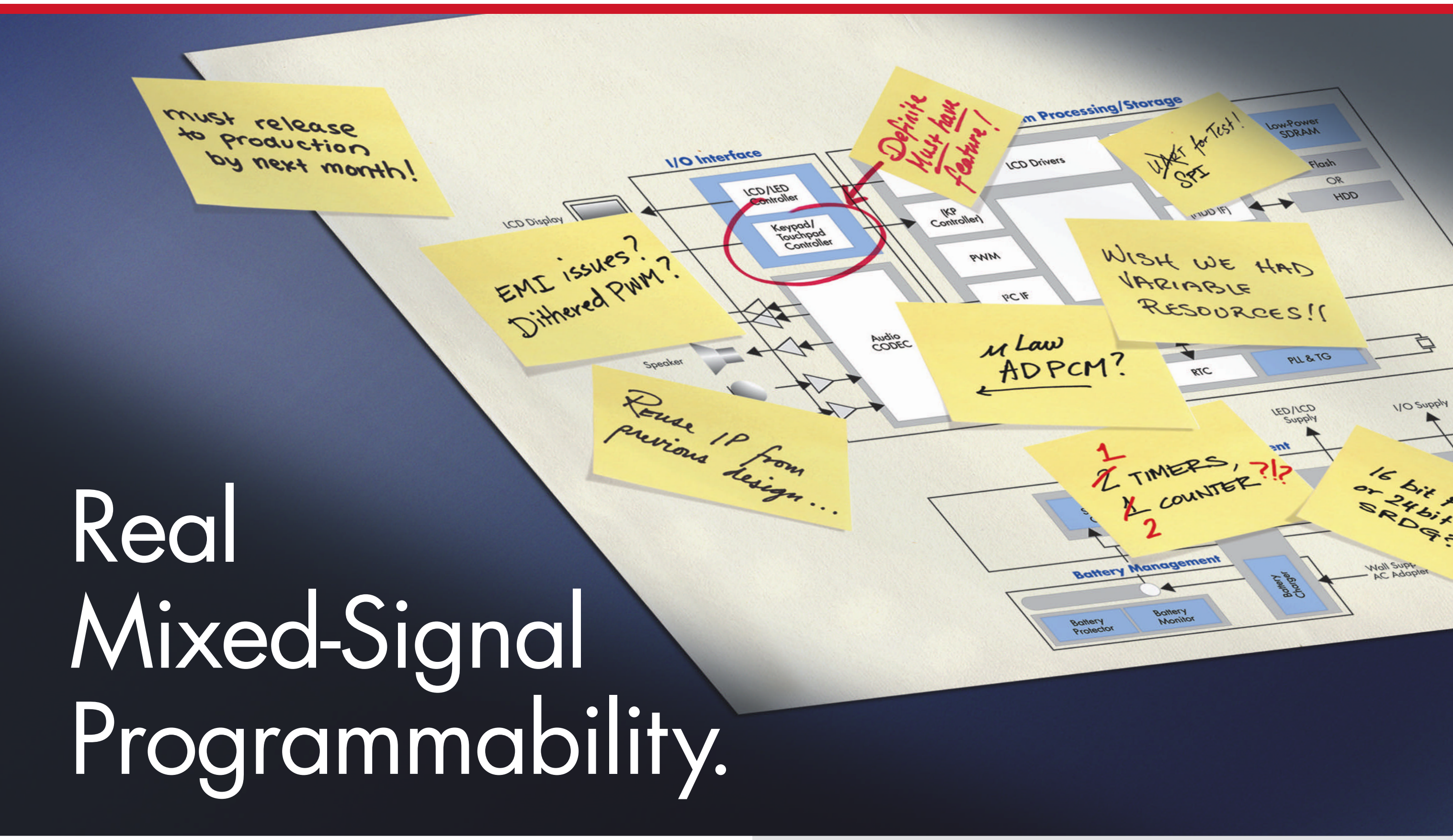
LOOKING AROUND

AT ADVANCED ENGINE-CONTROL TECHNOLOGY

Consumer electronics may still be getting all the press, but some of the most fascinating challenges in sensors, multiprocessing embedded systems, and real-time-software design are happening in another area altogether: engine control. Driven by increasingly stringent emissions standards and the surge of interest in alternative fuels, automotive-, truck-, and large-engine designers are finding that the engine controller is a critical component in any move to higher efficiency, lower emissions, or adaptation to new fuels. The days of carburetors, belt-driven valve timing, and mechanical distributors are over. The new era of electronically controlled multidose-fuel injection, electronically controlled valves, and intelligent integration of the entire power train is coming fast. And all those technologies grow from a foundation of real-time-embedded-system expertise.


TICKETS
SYSTEMS MAP

Real Mixed-Signal Programmability.



Get PSoC®. Because change happens.

PSoC flexibility enables changes anytime: at concept, through production, in the field. Specifications change constantly. Yet pressures to differentiate, minimize costs, and speed time-to-market remain the same. To stay ahead of the curve, you need flexibility, programmability, and scalability. PSoC's unique programmable architecture delivers this and more. Futureproof your design; make PSoC your agent of change.

PSoC delivers:

- The configurability of an FPGA, the mixed-signal integration of an ASIC, and the familiarity of an MCU.
- Reusable IP, compatible device families and variable resource options ensure you can optimize design efforts and accommodate changes.
- The industry's first visual embedded design tool, PSoC Express™, speeds design time, enabling you to generate a complete design without writing a single line of code.

GET STARTED WITH PSoC NOW.

- *Download our "Change Happens" White Paper and get 50%* off a PSoC development kit:* **www.cypress.com/changepaper**
- *Download free PSoC Express™ visual embedded software:* **www.cypress.com/changesoft**
- *Request free PSoC device samples:* **www.cypress.com/changechip**
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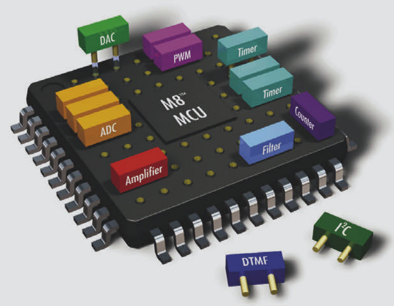

PSoC includes programmable analog and digital blocks, a fast MCU, flash and SRAM memory, all in a compact package (as small as 3mm x 3mm).

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PERFORM